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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD
DATE

<REV>

<ECN>

<ECO_DESCRIPTION>

<ECODATE>

MLB,D1,SCH (Preliminary_Test)

7/7/12

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
Preliminary_Test	1	SCHEM MLB D1	SCH	CRITICAL	
820-3190	1	PCBF MLB(NEW 2) D1	PCB	CRITICAL	

DRAWING

TITLE=MLB (NEW 2)

ABBREV=ABBREV

LAST MODIFIED=Thu May 10 09:19:18 2012

DRAWING TITLE

SCHEM,MLB,D1

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BOM Variants

[illegible]

Bar Code Labels / EEE #'s

[illegible]

Module Parts

[illegible]

D1 BOM GROUPS

[illegible]

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Alternate Parts

[illegible]

Alternate Parts


[illegible]

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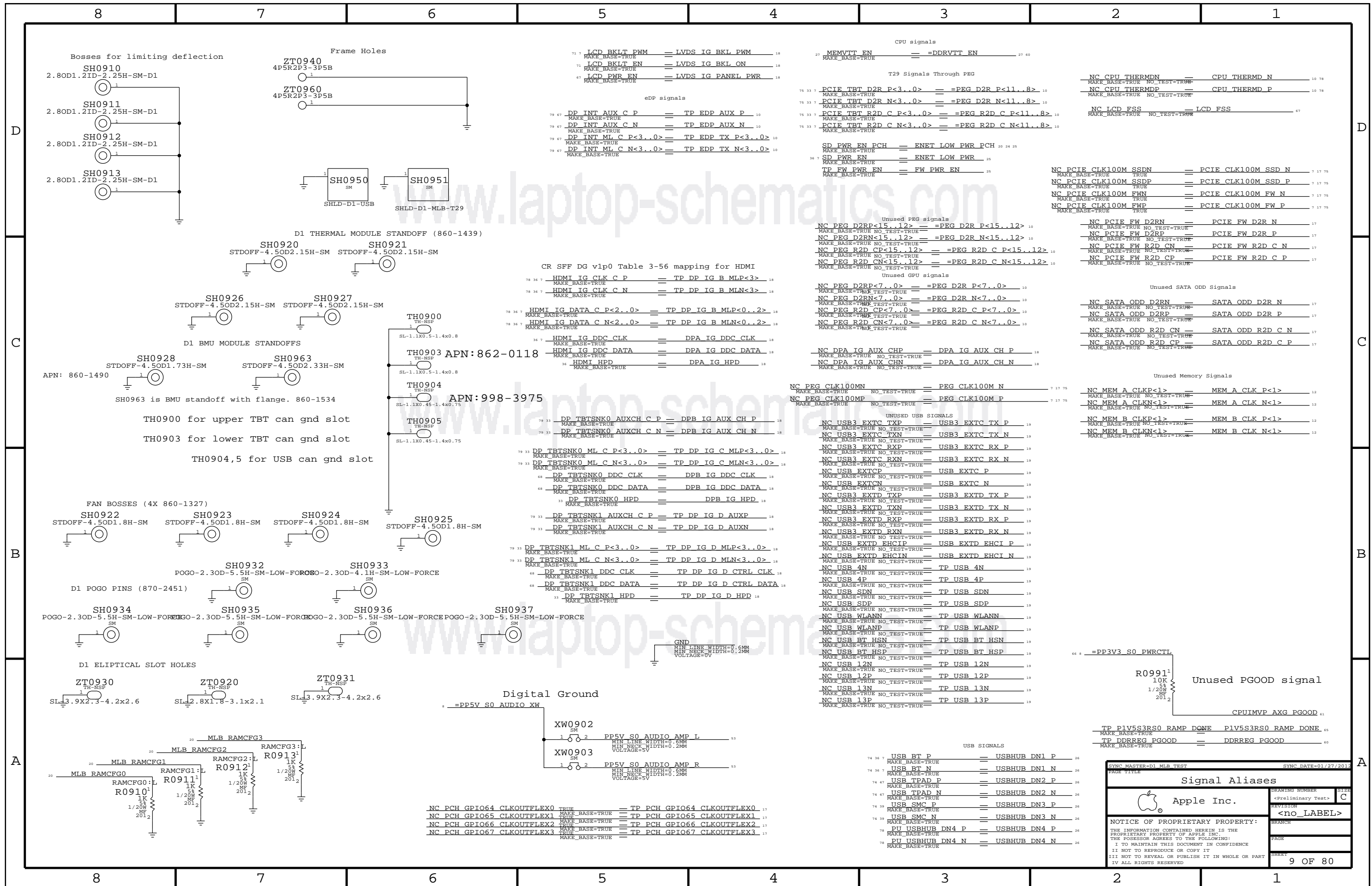
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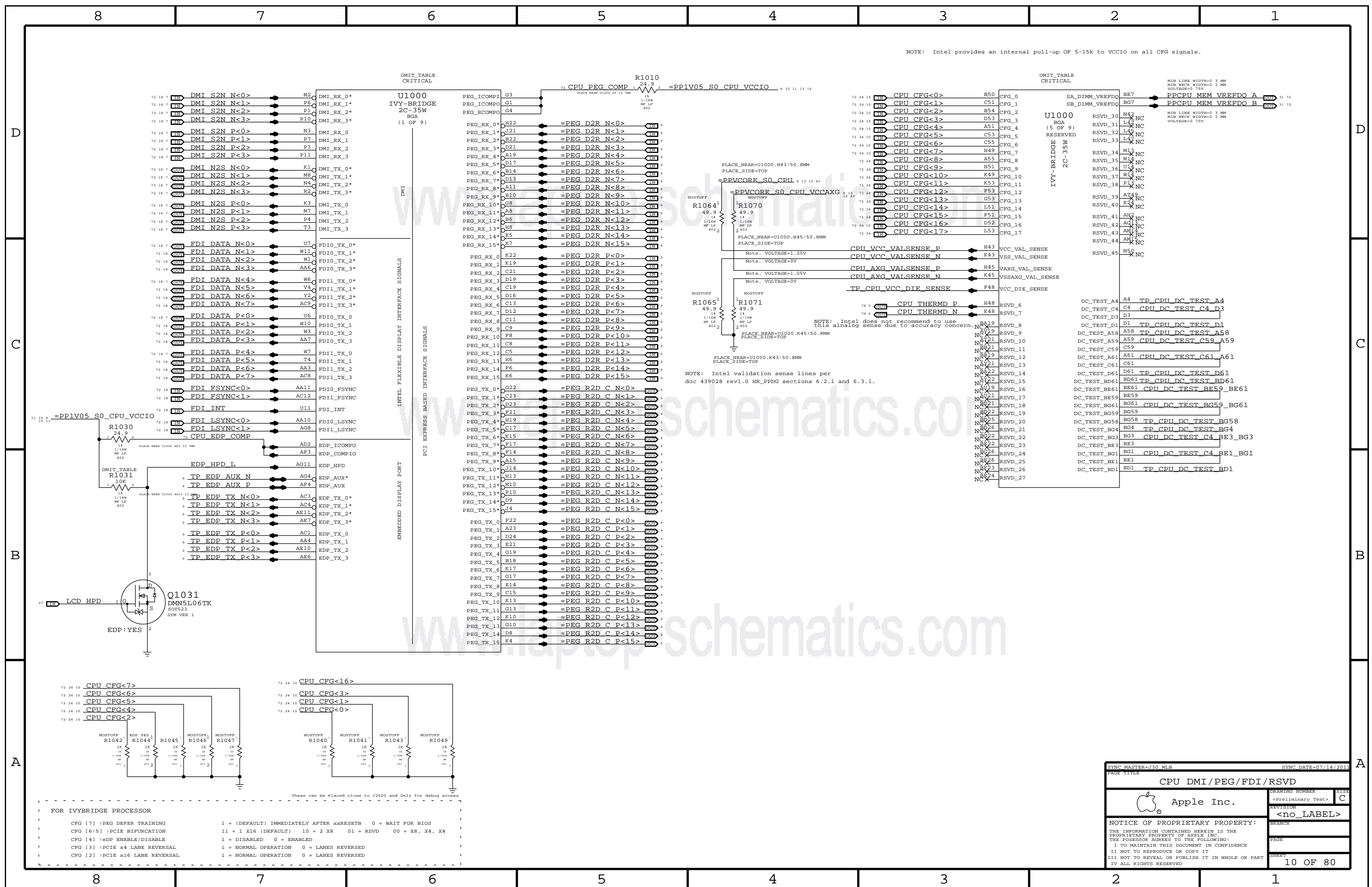
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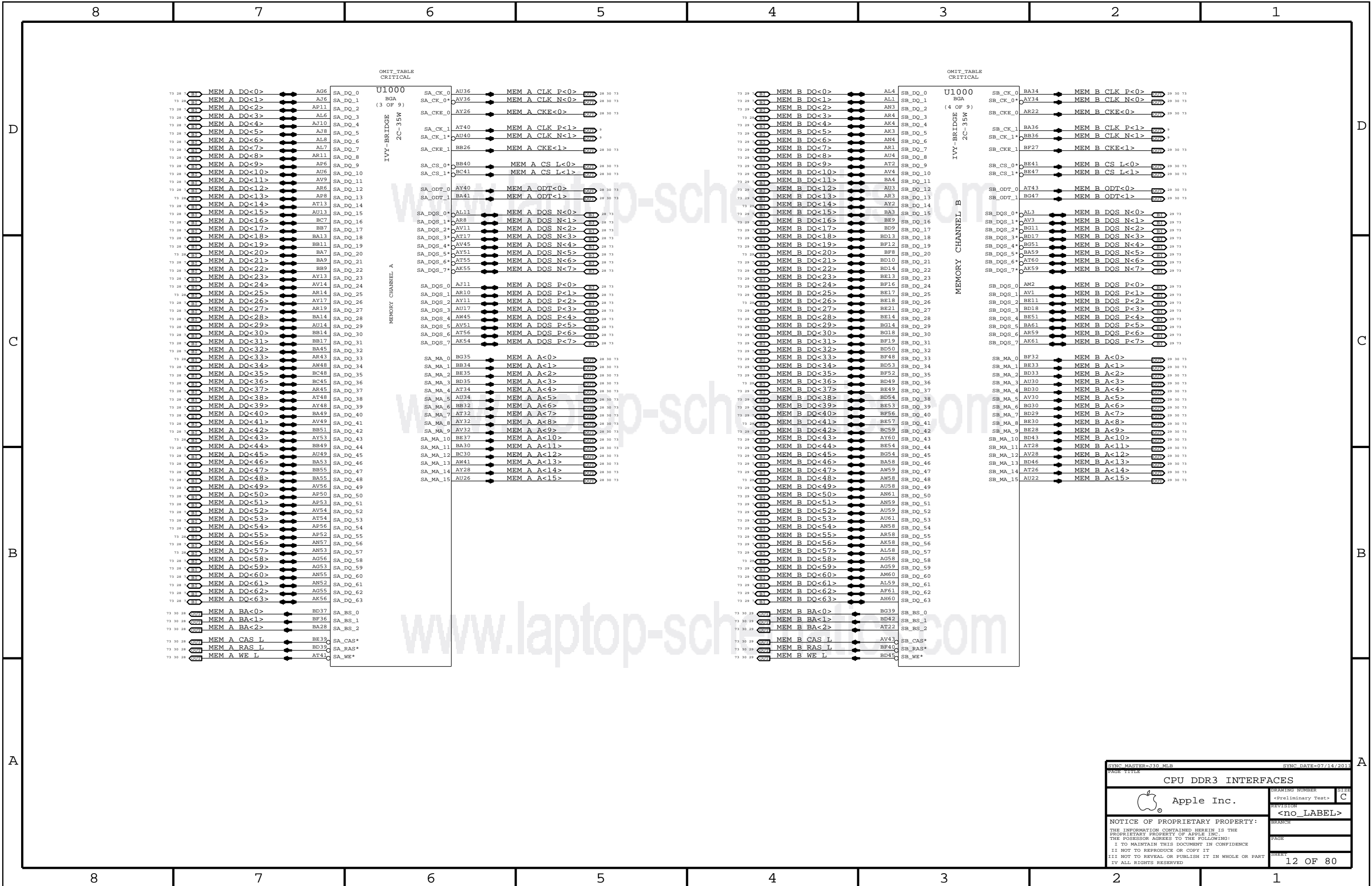
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J5650 (LEFT FAN CONN)		J5713 (KEY BOARD CONN)		CPU NO_TESTS		NC PCIE CAMERA D2RP	
FAN LT PWM		PP3V3 S4		TP TBT MONDC0		PCIE EXCARD D2R N	
FAN LT TACH		WS KBD1		TP TBT MONDC1		PCIE EXCARD D2R P	
J5660 (RIGHT FAN CONN)		WS KBD2		TP TBT PCIE RESET0 L		PCIE EXCARD R2D C N	
FAN RT PWM		WS KBD3		TP TBT PCIE RESET1 L		PCIE EXCARD R2D C P	
FAN RT TACH		WS KBD4		TP TBT PCIE RESET2 L		PCIE EXCARD R2D C N	
GND		WS KBD5		TP TBT PCIE RESET3 L		PCIE EXCARD R2D C P	
J3502 (ALS/CAMERA CONN)		WS KBD6		TP TBT XTAL25OUT		NC PCIE CLK100M CAMERAN	
SMBUS_SMC_2_S3_SDA		WS KBD7		TP DP TBTSRC ML CP<3>		PCIE CLK100M EXCARD N	
SMBUS_SMC_2_S3_SCL		WS KBD8		TP DP TBTSRC ML CN<3>		PCIE CLK100M EXCARD P	
PP5V S3 ALS/CAMERA F		WS KBD9		TP DP TBTSRC ML CP<2>		NC PCIE 5 D2RN	
J4400 (RIO CABLE CONN)		WS KBD10		TP DP TBTSRC ML CN<2>		NC PCIE 5 D2RP	
PP3V3 S4		WS KBD11		TP DP TBTSRC ML CP<1>		NC PCIE 5 R2D CN	
PP3V3 S3		WS KBD12		TP DP TBTSRC ML CN<1>		NC PCIE 5 R2D CP	
PP3V3 WLAN F		WS KBD13		TP DP TBTSRC ML CP<0>		NC PCIE 6 D2RN	
PP5V S4		WS KBD14		TP DP TBTSRC ML CN<0>		NC PCIE 6 D2RP	
PP1V5 S0		WS KBD15 CAP		TP DP TBTSRC ML CP<3>		NC PCIE 6 R2D CN	
J4410 (RIO FLEX CONN)		WS KBD16 NUM		TP DP TBTSRC ML CN<2>		NC PCIE 6 R2D CP	
USB EXT0 OC L		WS KBD17		TP DP TBTSRC ML CP<1>		NC PCIE 7 D2RN	
HDMI IG DDC CLK		WS KBD18		TP DP TBTSRC ML CN<1>		NC PCIE 7 D2RP	
HDMI IG DDC DATA		WS KBD19		TP DP TBTSRC ML CP<0>		NC PCIE 7 R2D CN	
HDMI HPD L		WS KBD20		TP DP TBTSRC ML CN<0>		NC PCIE 7 R2D CP	
PM SLP S3 L		WS KBD21		TP SPI CS1 L		NC PCIE 8 D2RN	
PM SLP S4 L		WS KBD22		TP PCH GPIO8		NC PCIE 8 D2RP	
AP CLKREO O L		WS KBD ONOFF L		TP PCH STRP BBS1		NC PCIE 8 R2D CN	
ENET RESET L		WS LEFT SHIFT KBD		TP PCH STRP ESI L		NC PCIE 8 R2D CP	
ENET CLKREO L		WS LEFT OPTION KBD		TP PCH TP23		NC PCIE CLK100M PE4N	
SD PWR EN		WS CONTROL KBD		TP PCI CLK33M OUT2		NC PCIE CLK100M PE4P	
SDCONN STATE CHANGE_SMC		J5700 (TPD FLEX CONN)		TP PCIE CLK100M PEGAN		NC PCIE CLK100M PEBN	
PCIE WAKE L		PP3V3 S4		TP PCIE CLK100M PEGAP		NC PCIE CLK100M PEBP	
AP CLKREO O L		Z2 CS L		TP PM SLP A L		TP SATA C D2RN	
AP RESET CONN L		Z2 MISO		TP PVOUT PCH DCPUSBY		TP SATA C D2RP	
WIFI EVENT L		Z2 SCLK		TP SMC MP55 LED PWR		TP SATA C R2D CN	
USB EXT0 P		Z2 HOST INTN		TP SMC MP55 LED CHG		TP SATA C R2D CP	
USB EXT0 N		PP5V S4 CUMULUS		TP SMS INT2		TP SATA D D2RN	
USB BT CONN P		Z2 CLKIN		PCIE TBT R2D C P<3..0>		TP SATA D D2RP	
USB BT CONN N		SMBUS_SMC_2_S3_SCL		PCIE TBT R2D C N<3..0>		TP SATA D R2D CN	
AP RESET CONN L		SMBUS_SMC_2_S3_SDA		PCIE TBT R2D P<3..0>		TP SATA D R2D CP	
SMBUS_PCH_CLK		PSOC SCLK		PCIE TBT D2R C P<3..1>		TP SATA E D2RN	
SMBUS_PCH_DATA		PSOC MOSI		PCIE TBT D2R C N<3..1>		TP SATA E D2RP	
SMBUS_SMC_1_S0_SCL		PSOC MISO		PCIE TBT D2R N<3..1>		TP SATA E R2D CN	
SMBUS_SMC_1_S0_SDA		RICKB L		MEM A DO<0>		TP SATA E R2D CP	
J5815 (KBD BACKLIGHT CONN)		PSOC P_CS L		MEM A DO<1..2>		TP CRT IG BLUE	
PP_KBD_BOOST_VOUT		Z2 KEY ACT L		MEM A DO<19..14>		TP CRT IG GREEN	
KBDLED_CATHODE1		J6900 (DC POWER CONN)		MEM A DO<24..21>		TP CRT IG RED	
KBDLED_CATHODE2		ADAPTER SENSE		MEM A DO<32..26>		TP CRT IG DDC CLK	
SMC_KBDLED_PRESENT L		PI8V5 DCIN FUSE		MEM A DO<42..34>		TP CRT IG DDC DATA	
J6950 (MAIN BATT CONN)		GND		MEM A DO<54..44>		TP CRT IG HSYNC	
PPVBAT G3H CONN		J4500 (SSD/HDD FLEX CONN)		MEM A DO<63..58>		TP CRT IG VSYNC	
SMBUS_SMC_5_G3_SCL		PP3V3 S0 SSD FLT		MEM B DO<2..0>		TP HDA SDIN1	
SMBUS_SMC_5_G3_SDA		SMC_OOB1_TX L		MEM B DO<13..4>		TP HDA SDIN2	
SYS_DETECT L R		SMC_OOB1_RX L		MEM B DO<19..15>		TP HDA SDIN3	
SYS_DETCT L R		PP5V S0 HDD FLT		MEM B DO<25..21>		TP SDVO TVCLKINN	
SYSDET1		GND		MEM B DO<35..27>		TP SDVO TVCLKINP	
SYSDET 3_4		J5100 (LPC + SPI CONN)		MEM B DO<40..37>		TP SDVO STALLN	
J6801 (2 MIC CONN)		PP3V42 G3H		MEM B DO<47..42>		TP SDVO STALLP	
CON_DMIC_PWR		PP5V S0		MEM B DO<57..49>		TP SDVO INTN	
CON_DMIC_SDA1		LPC_CLK33M LPCPLUS		MEM B DO<63..59>		TP SDVO INTP	
CON_DMIC_CLK		LPC_AD<0>		NC MEM EVENT L		TP PCI PME L	
J6900 (EDP CONN)		LPC_AD<1>		HDMI IG CLK C P		TP PCI CLK33M OUT3	
PP5VR3V3 SW_LCD		LPC_AD<2>		HDMI IG CLK C N		TP AUD MIC INRP	
PPVOUT S0 LCDBKLT		LPC_AD<3>		HDMI IG DATA C P<2..0>		TP AUD MIC INRN	
LED_RETURN 6		LPC_AD<4>		HDMI IG DATA C N<2..0>		AUD SPDIF IN	
LED_RETURN 5		SPI_ALT_MOSI		PCIE AP D2R P		TP BKL FAULT	
LED_RETURN 4		LPCPLUS_GPIO		PCIE AP D2R N		TP LPC DREQ0 L	
LED_RETURN 3		LPCPLUS_RESET L		PCIE AP R2D P		TP CLINK CLK	
LED_RETURN 2		SMC_TDO		PCIE AP R2D N		TP CLINK DATA	
LED_RETURN 1		TP_SMC_TRST L		TP XDP PCH HOOK4		TP CLINK RESET L	
LCD_HPD CONN		TP_SMC_MDI		TP XDP PCH HOOK5		TP CLINK RESET L	
J3401 & J3402 (AIRPORT/BT/CAMERA CONN)		SMC_TX L		TP XDP PCH OBSFN B<0>		TP CLINK RESET L	
PCIE_CLK100M_AP_CONN_P		SPI_ALT_MISO		TP XDP PCH OBSFN B<1>		TP CLINK RESET L	
PCIE_CLK100M_AP_CONN_N		LPC_FRAME L		TP XDP PCH OBSFN A<0>		TP CLINK RESET L	
AP_CLKREQ O L		SPIROM_USE_MLB		TP XDP PCH OBSFN A<1>		TP CLINK RESET L	
AP_RESET CONN L		PM_CLKRUN L		TP XDP PCH OBSFN D<0>		TP CLINK RESET L	
PP5V S3 USB A F		SPI_ALT_CS L		TP XDP PCH OBSFN D<1>		TP CLINK RESET L	
USB LT1 N		LPC_SERI0		TP XDP PCH TRST L		TP CLINK RESET L	
USB LT1 P		LPC_PWDWN L		TP XDP PCH TRST N		TP CLINK RESET L	
GND		SMC_TCK		TP XDP PCH TRST L		TP CLINK RESET L	
GND		SMC_TDI		TP XDP PCH TRST N		TP CLINK RESET L	
GND		SMC_RESET L		TP XDP PCH TRST L		TP CLINK RESET L	
GND		SMC_ROMBOOT		TP XDP PCH TRST N		TP CLINK RESET L	
GND		SMC_RX L		TP XDP PCH TRST L		TP CLINK RESET L	
GND		SMC_TMS		TP XDP PCH TRST N		TP CLINK RESET L	
GND		GND		TP XDP PCH TRST L		TP CLINK RESET L	
GND		GND		TP XDP PCH TRST N		TP CLINK RESET L	
GND		GND		TP XDP PCH TRST L		TP CLINK RESET L	
GND		GND		TP XDP PCH TRST N		TP CLINK RESET L	
GND		GND		TP XDP PCH TRST L		TP CLINK RESET L	
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GND		GND		TP XDP PCH TRST N		TP CLINK RESET L	
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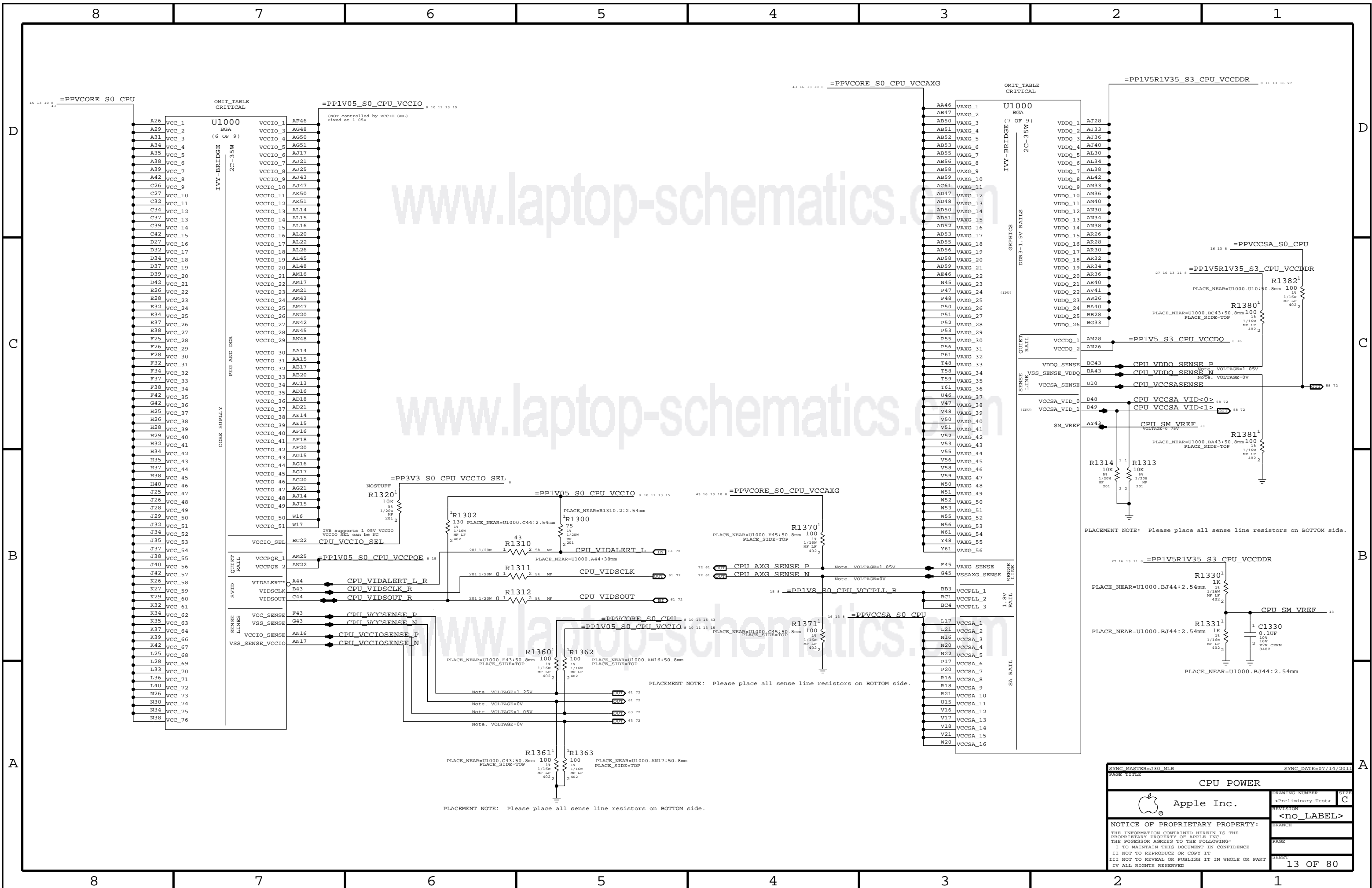





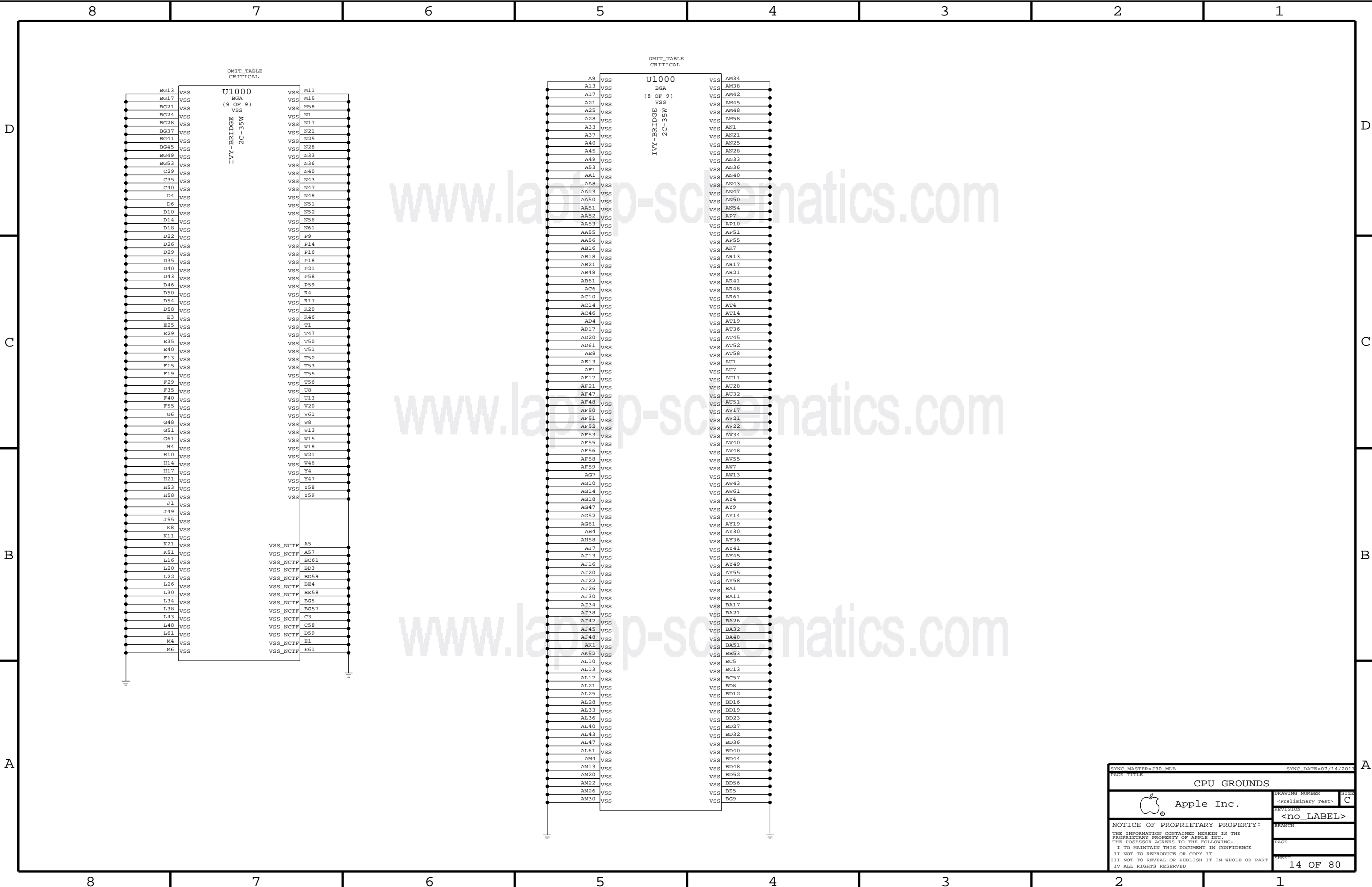




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CPU GROUNDS

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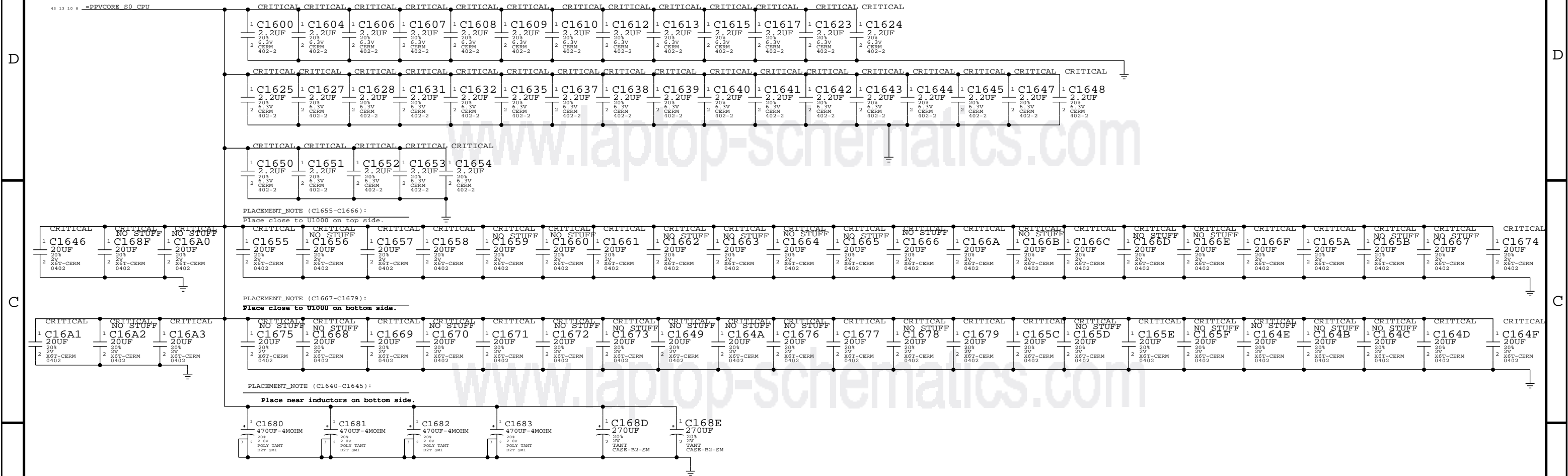
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CPU VCORE DECOUPLING

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

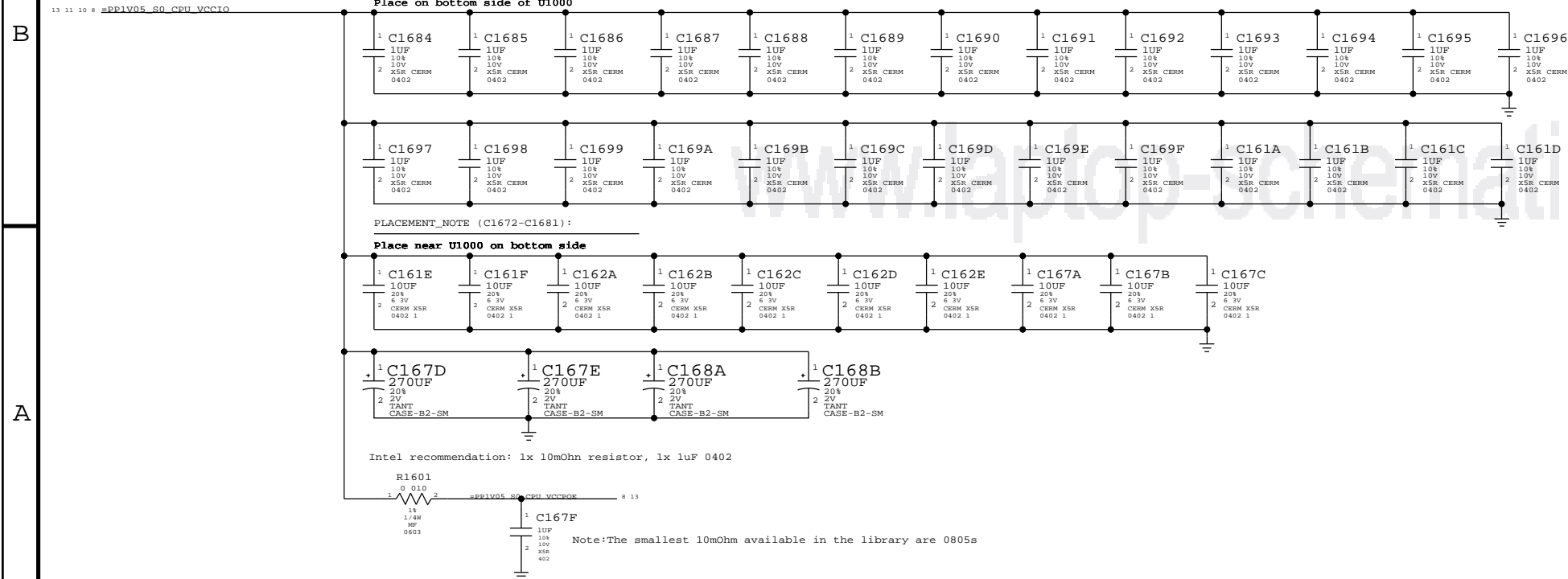


CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

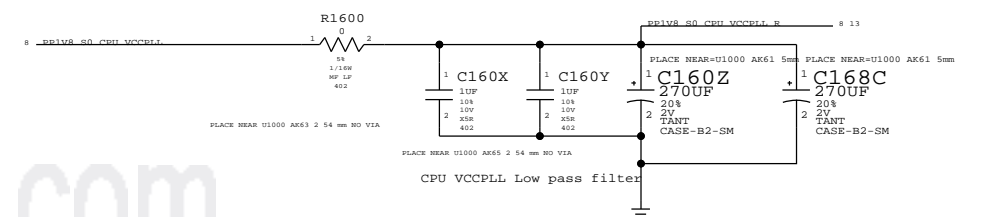
Place on bottom side of U1000




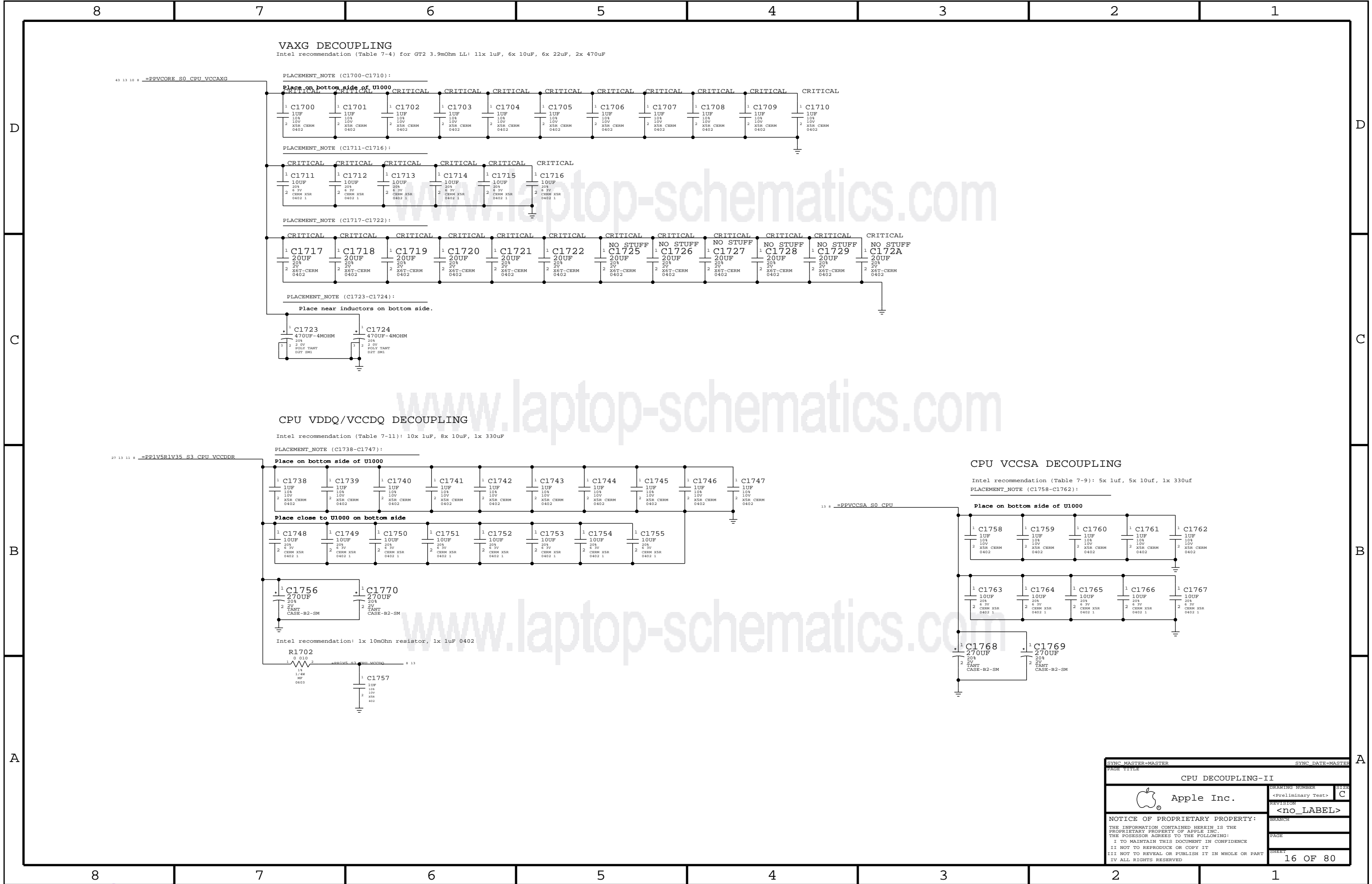
CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):



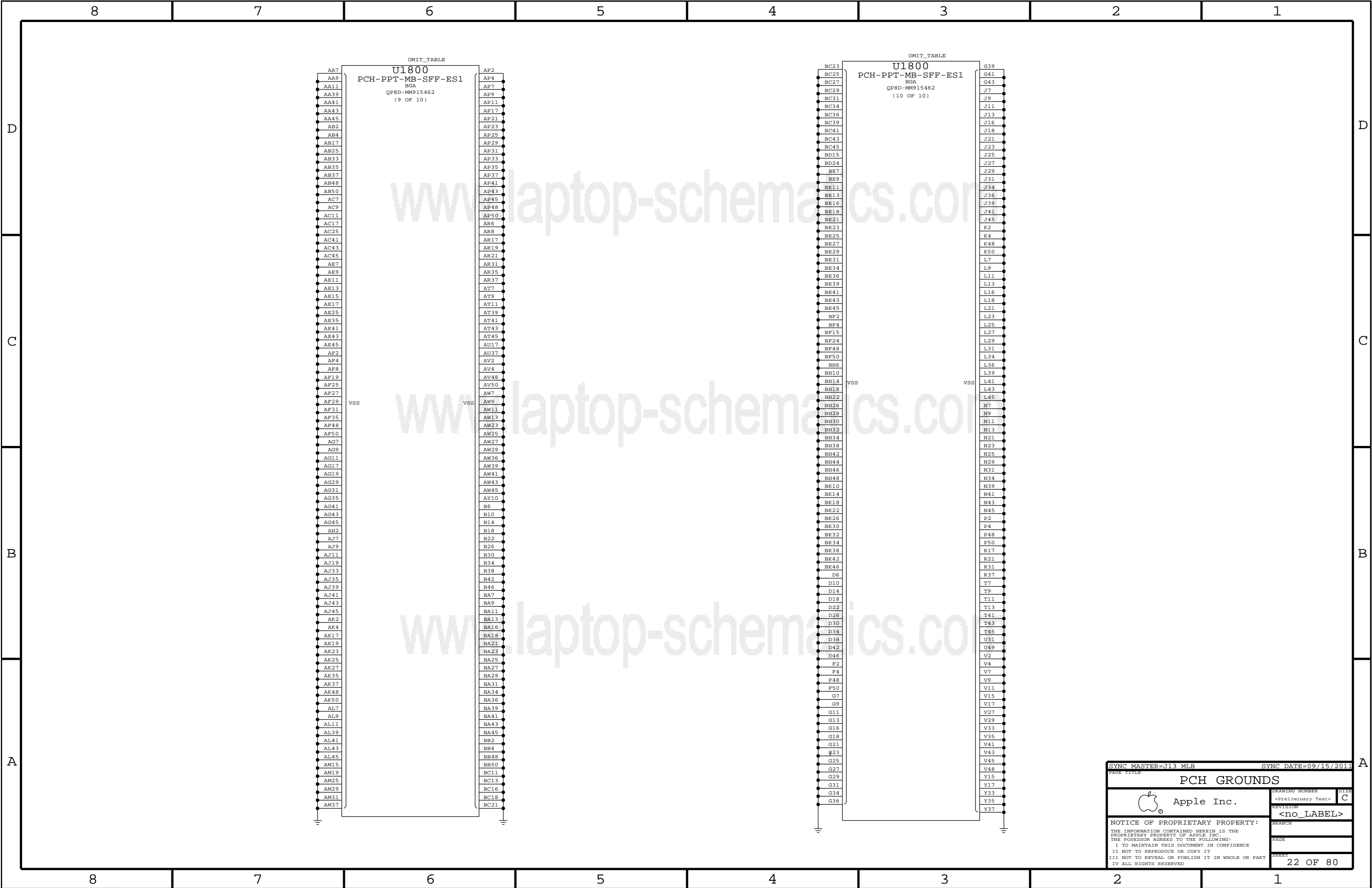
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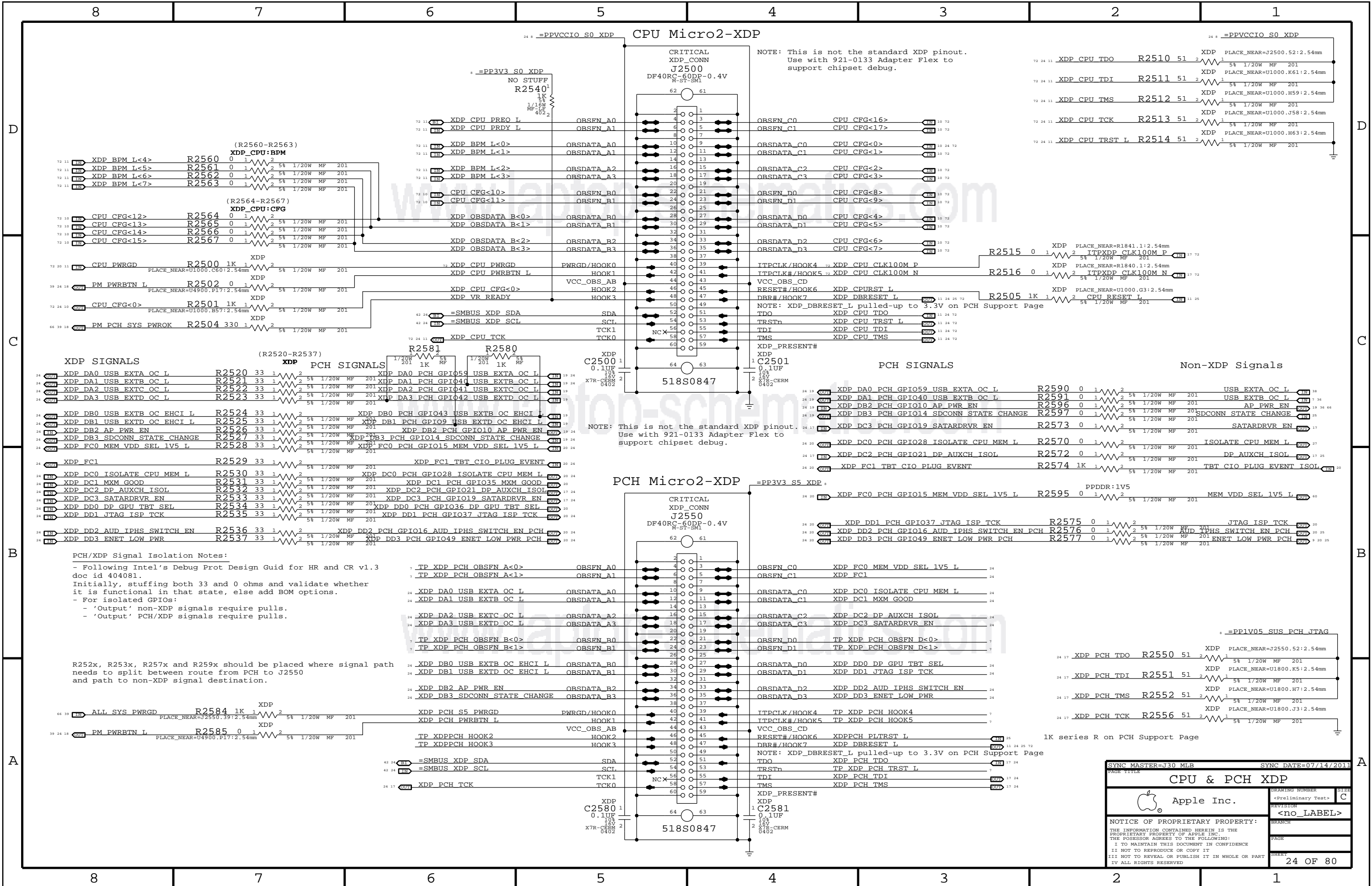












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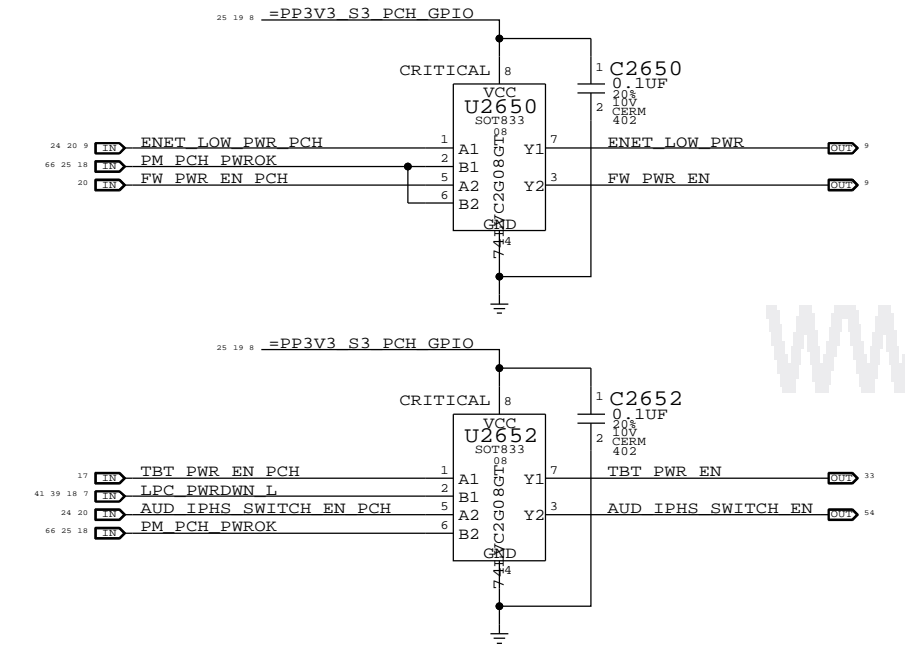
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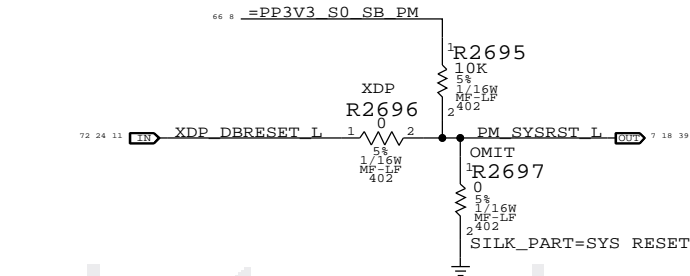
B

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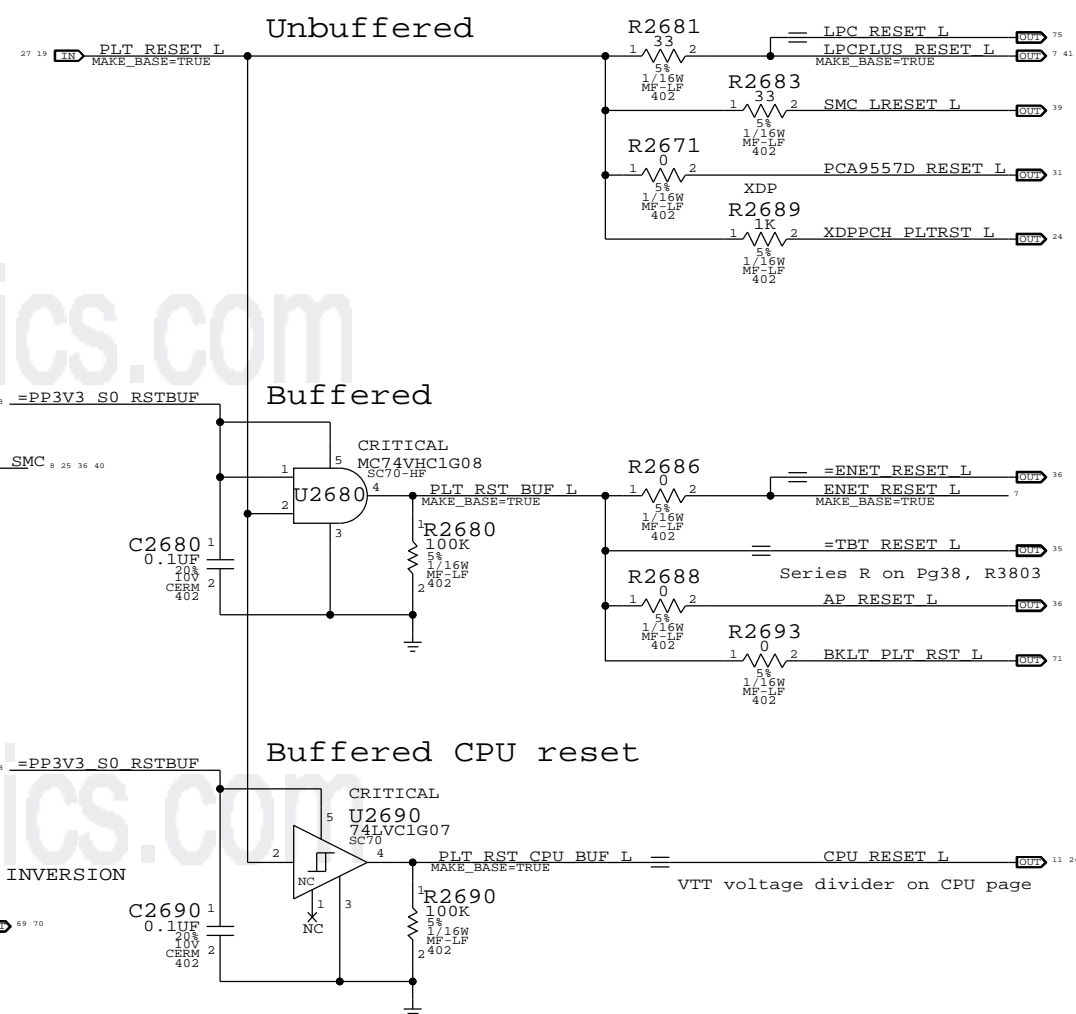
GPIO Glitch Prevention



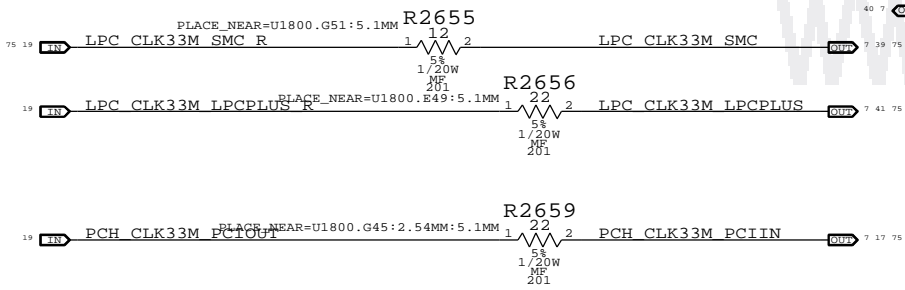
PCH Reset Button



Platform Reset Connections



33 MHz Clock Series Termination

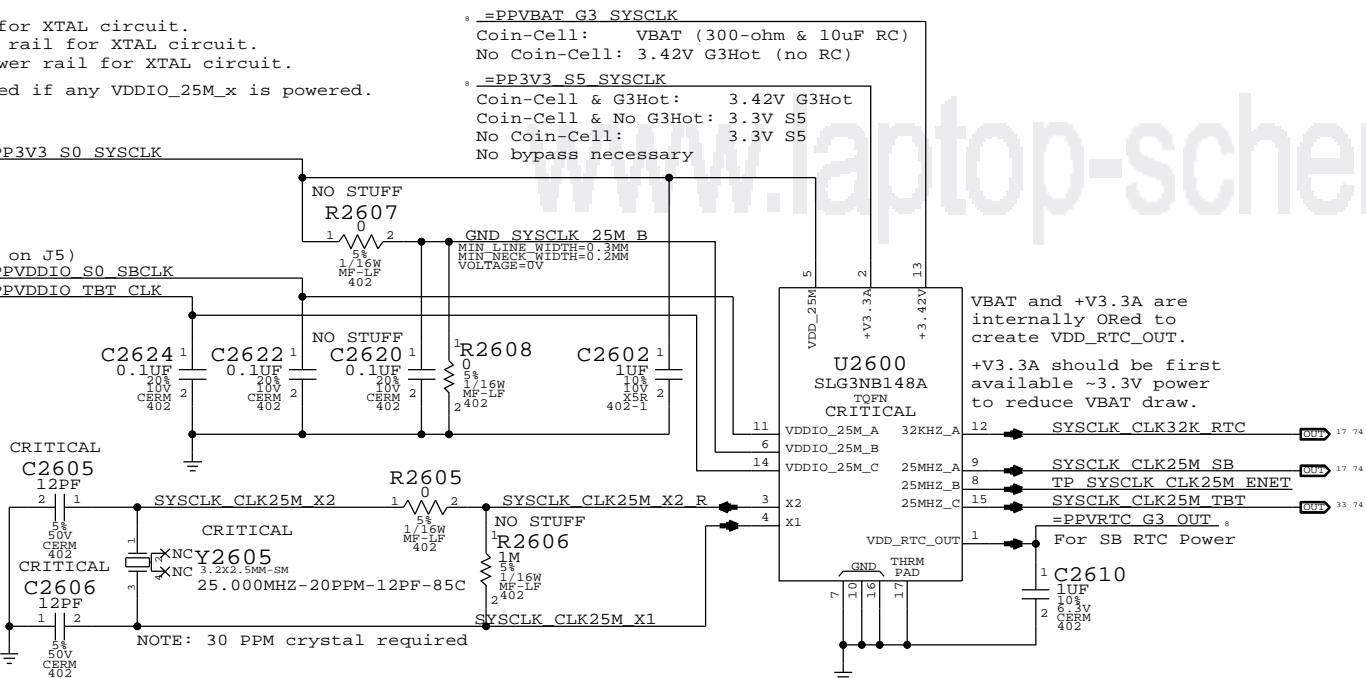


System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

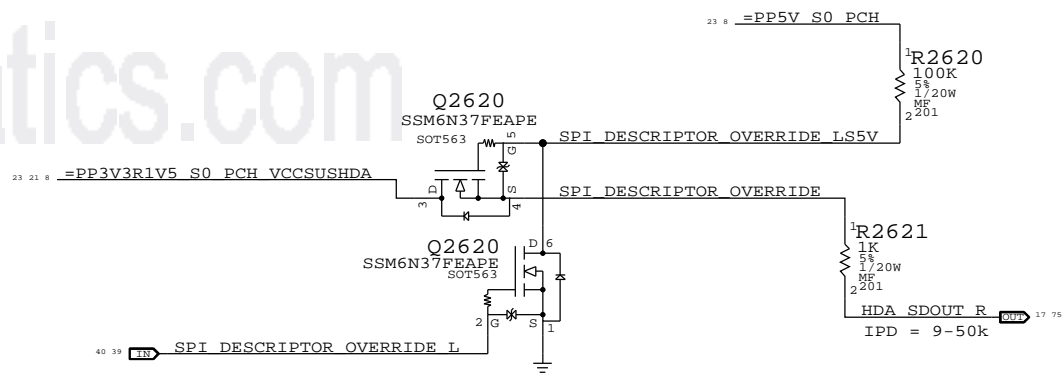
GreenClk 25MHz Power =PP3V3 S0 SYSCLK


Ethernet XTAL Power (Unused on J5)
SB XTAL Power =PPVDDIO S0 SBCLK
TBT XTAL Power =PPVDDIO TBT CLK

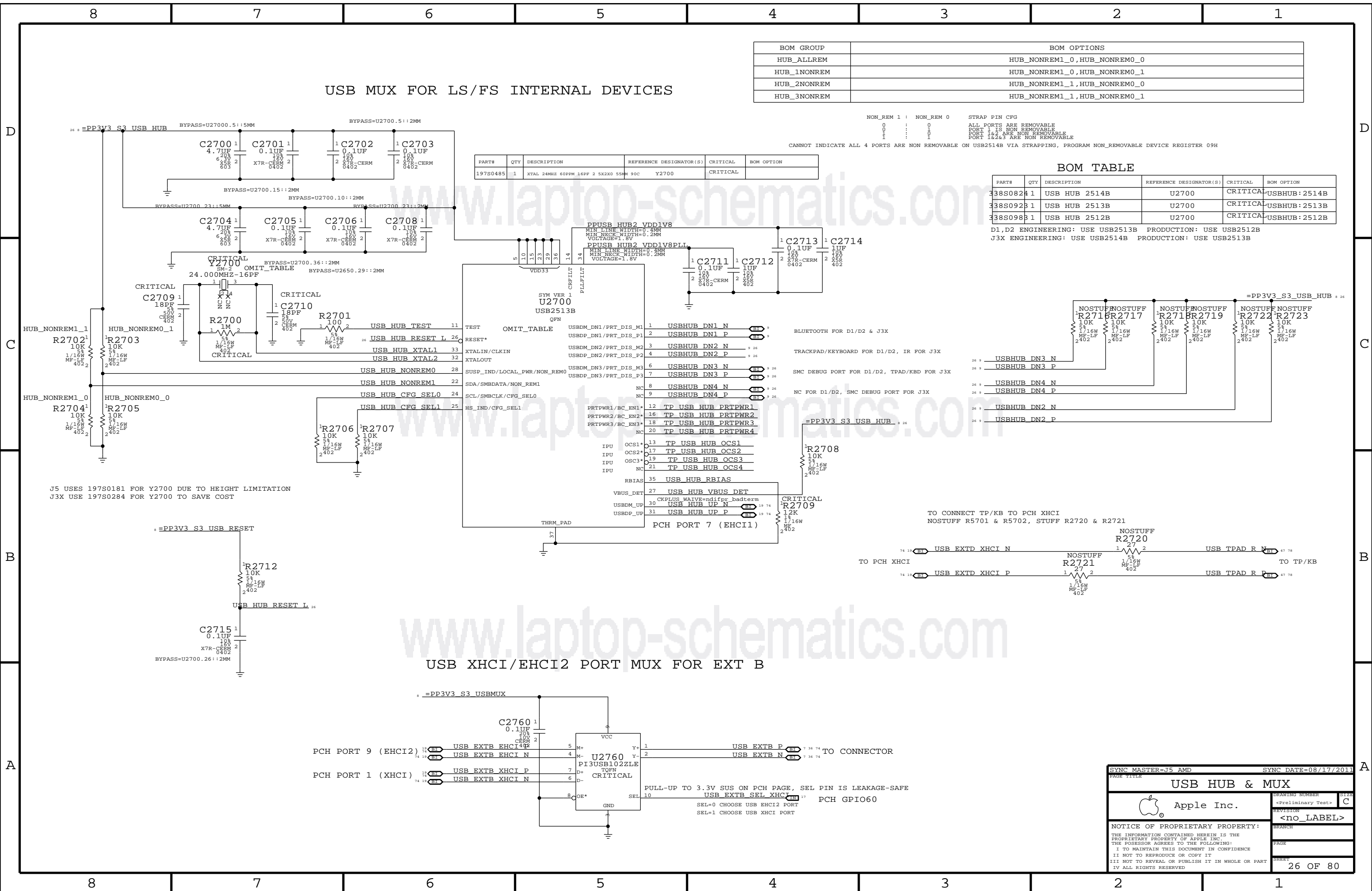


PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Chipset Support			
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

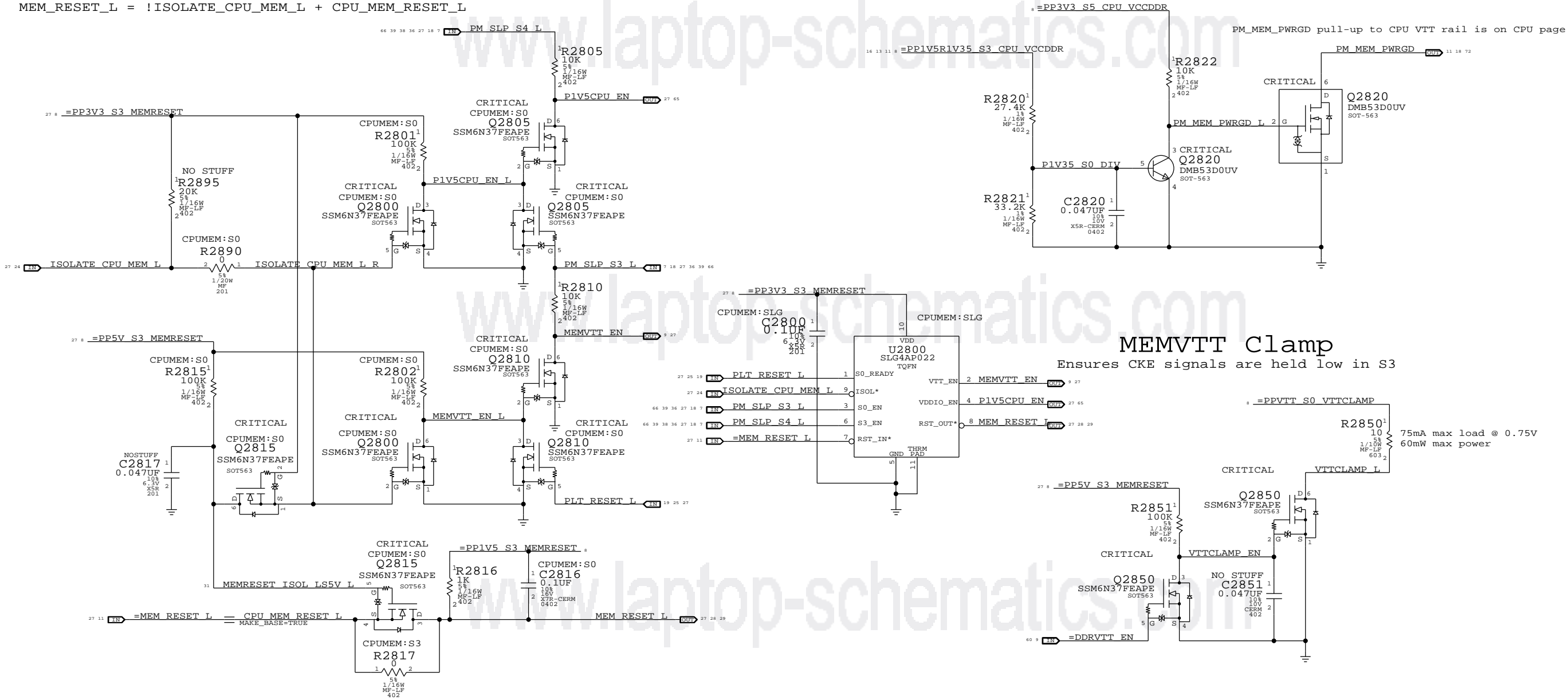
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L


1V35 S0 "PGOOD" for CPU



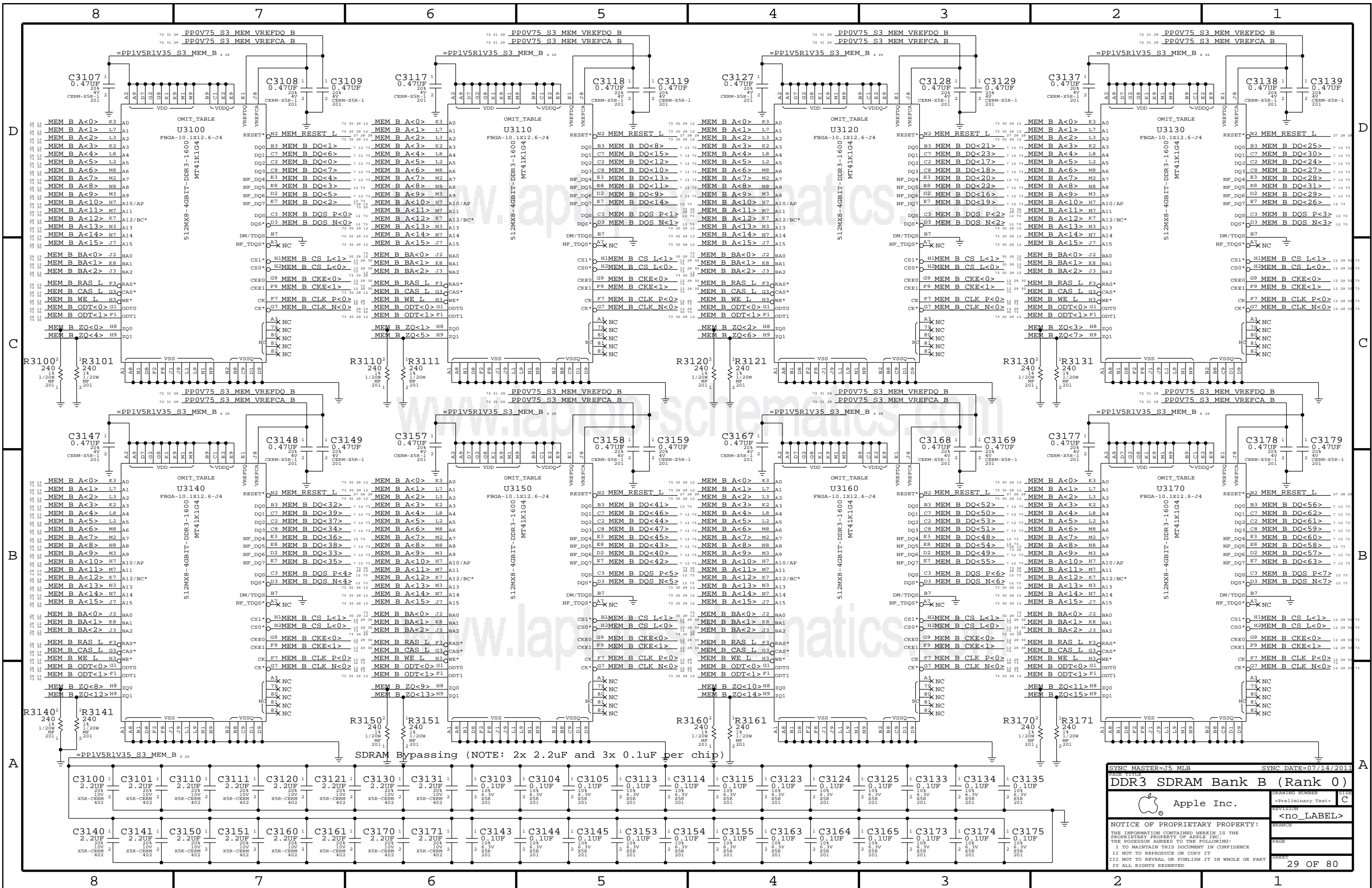
Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

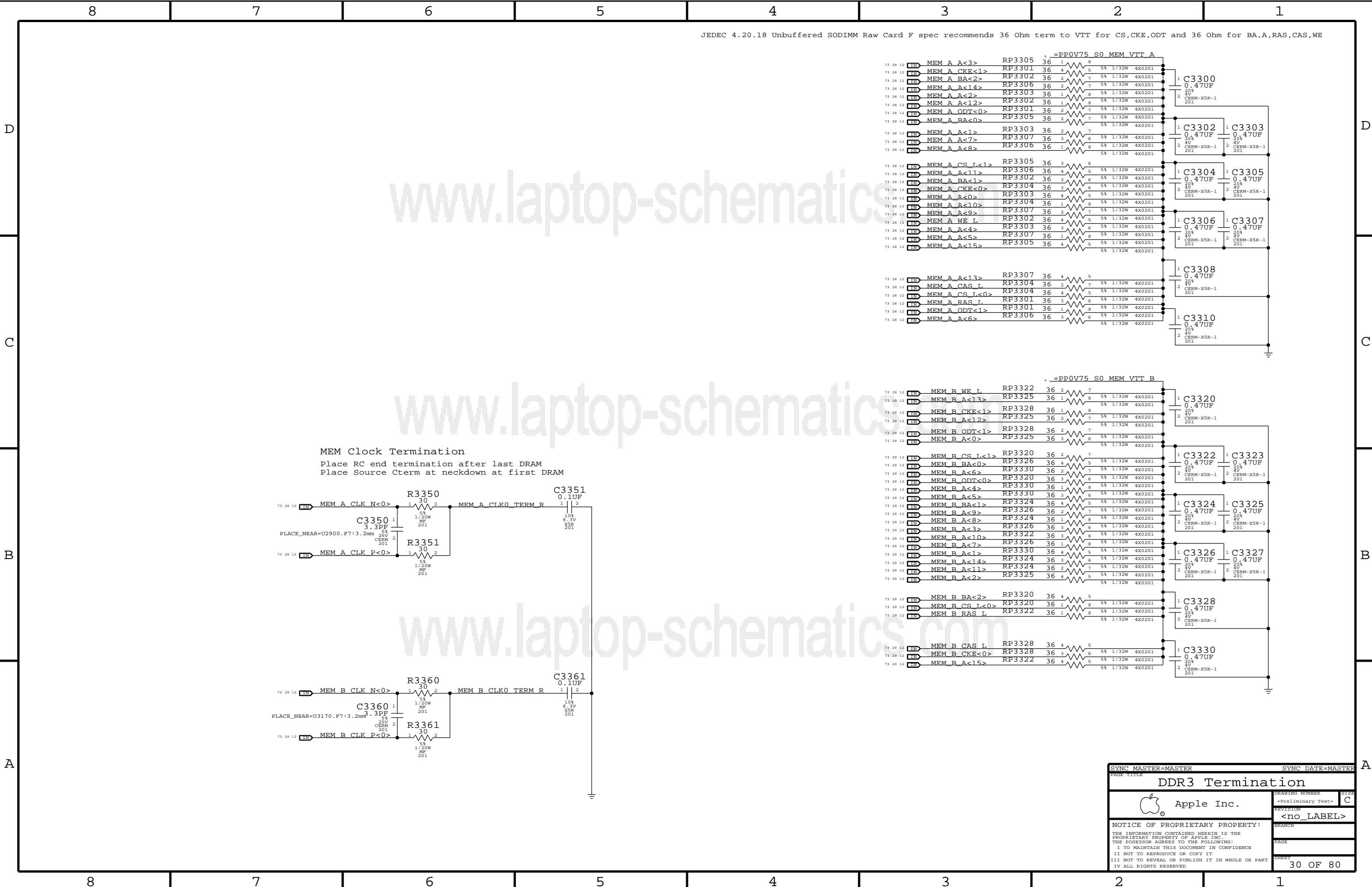
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=J5 MLB		SYNC DATE=07/29/2011	
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CPU Memory S3 Support		DRAWING NUMBER	
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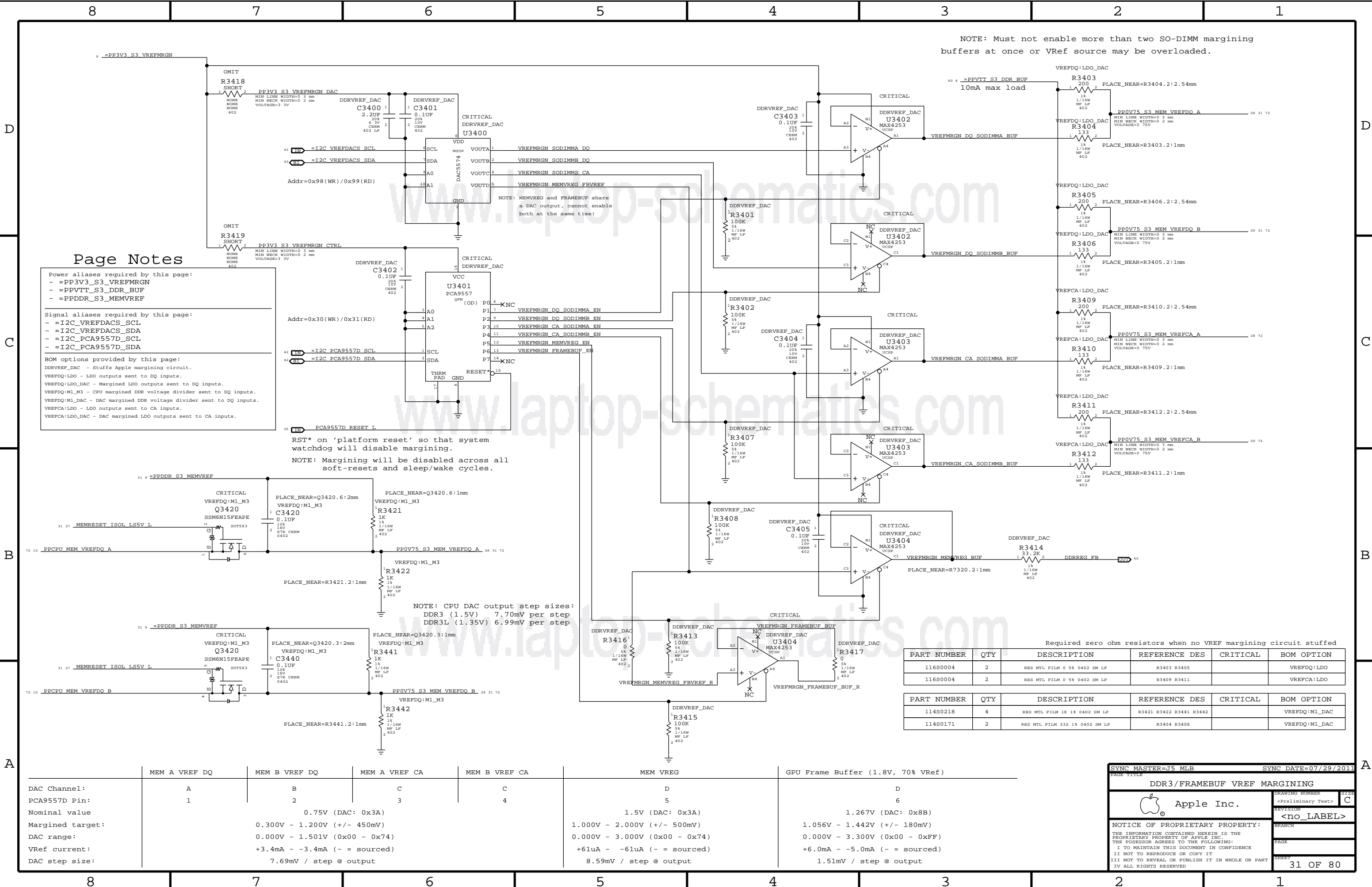






MEM Clock Termination
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

SYNC MASTER=MASTER		SYNC DATE=MASTER	
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DDR3 Termination			
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES MTL FILM 0 5% 0402 SM LF	R3403 R3405		VREFDQ:LDO
116S0004	2	RES MTL FILM 0 5% 0402 SM LF	R3409 R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES MTL FILM 1K 1% 0402 SM LF	R3421 R3422 R3441 R3442		VREFDQ:M1_DAC
114S0171	2	RES MTL FILM 332 1% 0402 SM LF	R3404 R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (= sourced)			+61uA - -61uA (= sourced)	+6.0mA - -5.0mA (= sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

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518S0767

CRITICAL
J3502
819Q-3506-K281
F-RT-SM

ALS

=I2C ALS SDA

=I2C ALS SCL

=PP5V_S3_ALSCAMERA_F

=USB_CAMERA_CONN_N

=USB_CAMERA_CONN_P

CAMERA

MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=5V

CRITICAL

L3507

90-OHM

DLFONS

PLACE NEAR J3502 2 2 5400H

USB CAMERA N

USB CAMERA P

PLACE NEAR J3502 4 2 5400H

L3508

FERR-120-OHM-1.5A

0402-LF

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C3552

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
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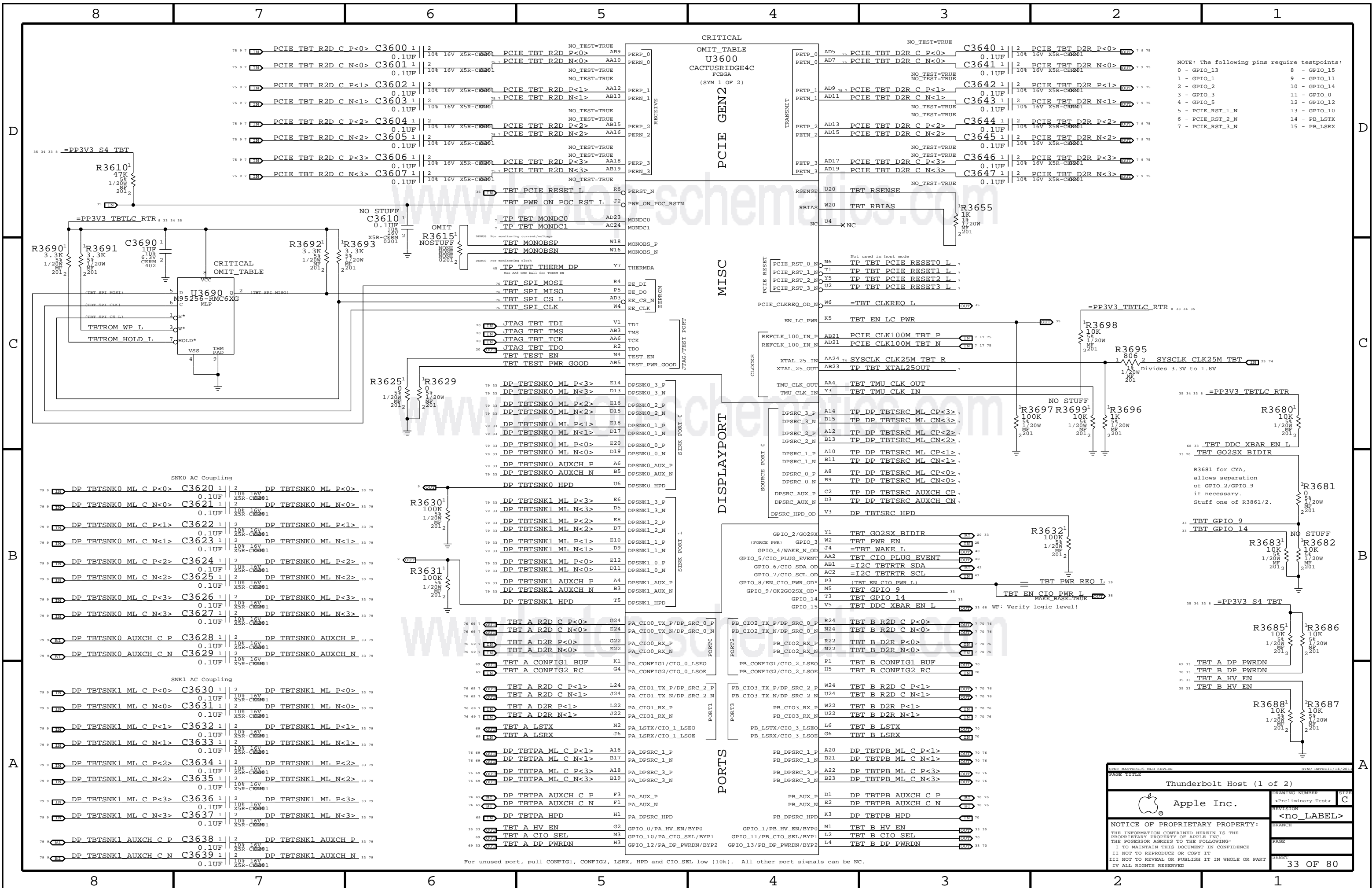
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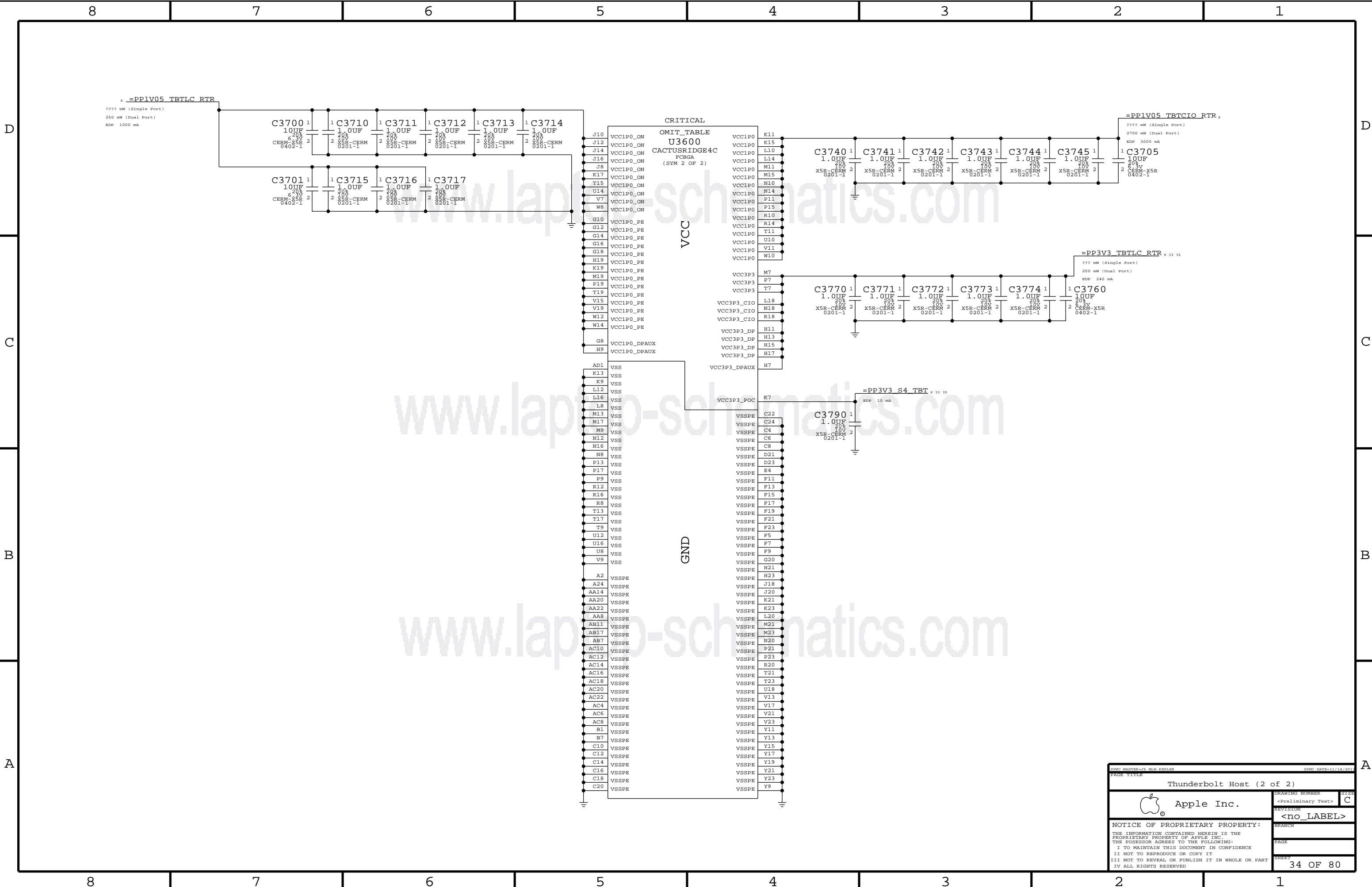
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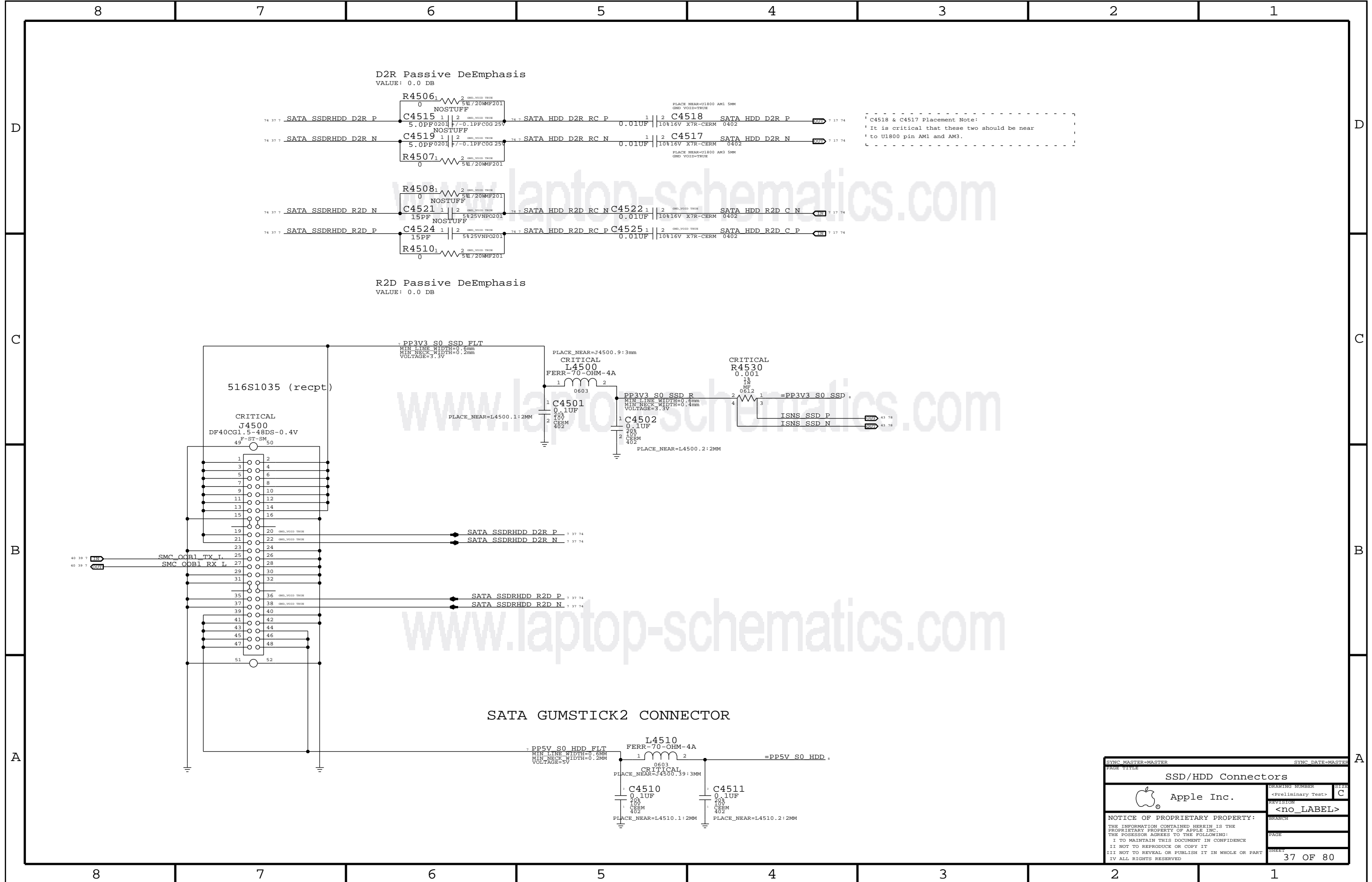
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
ALS/CAMERA CONNECTOR			
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		<Preliminary Test>	
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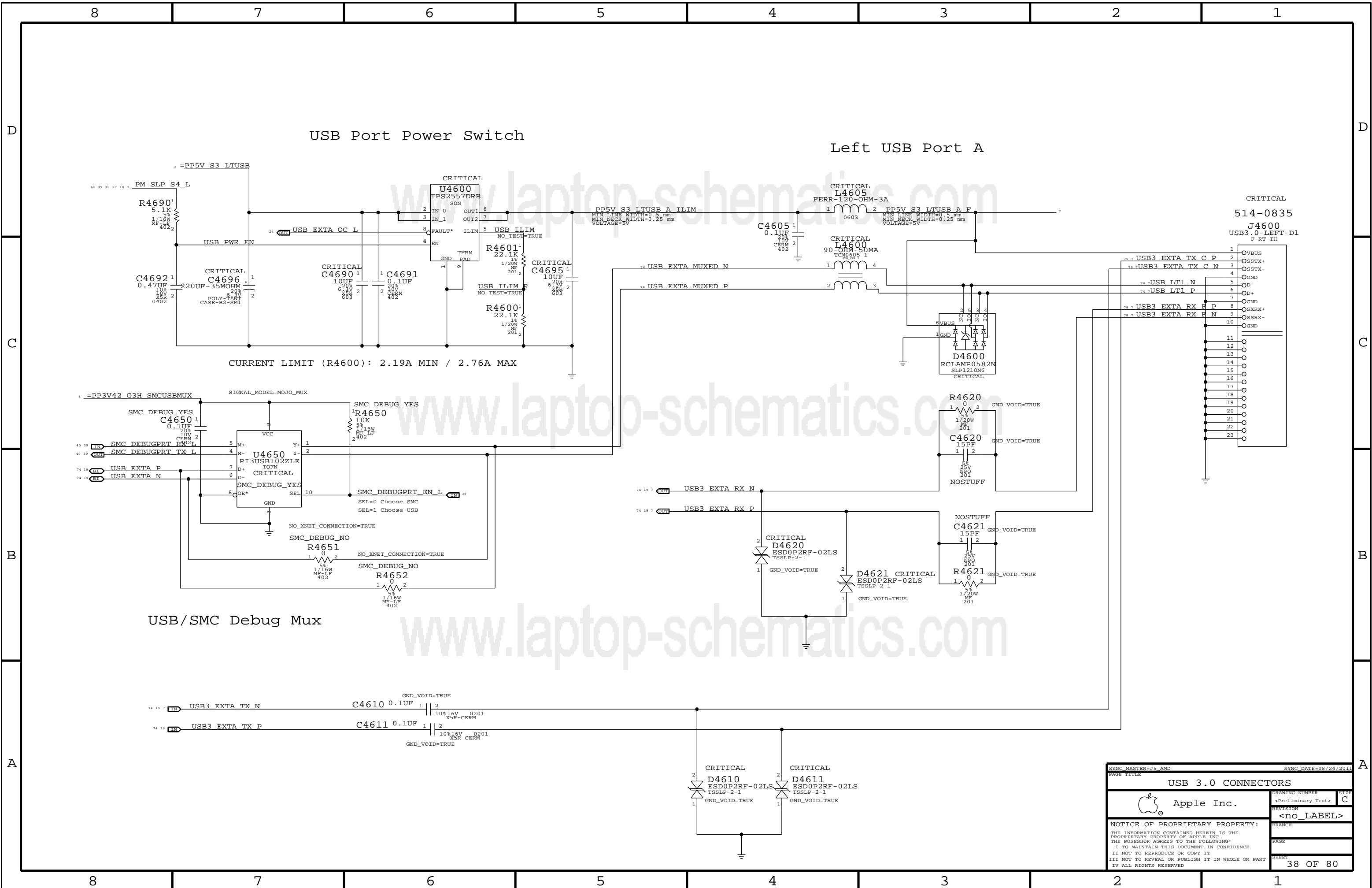




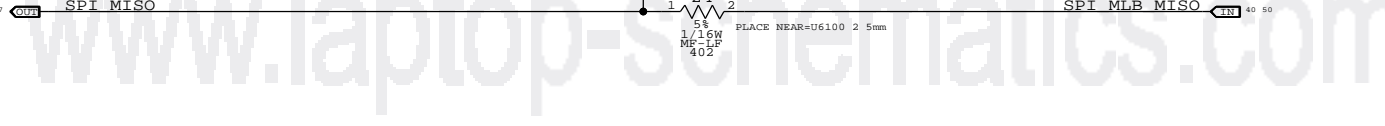




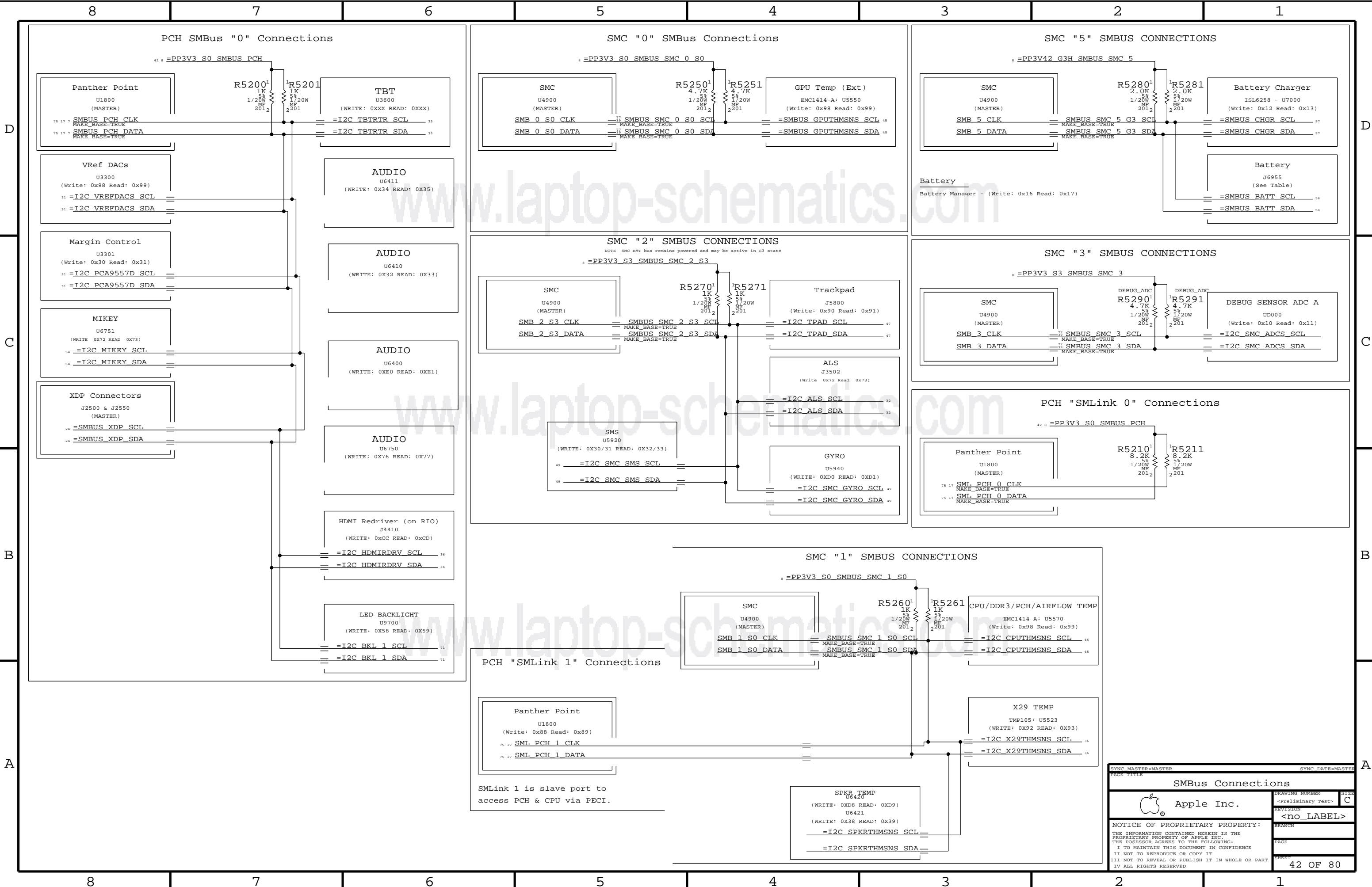
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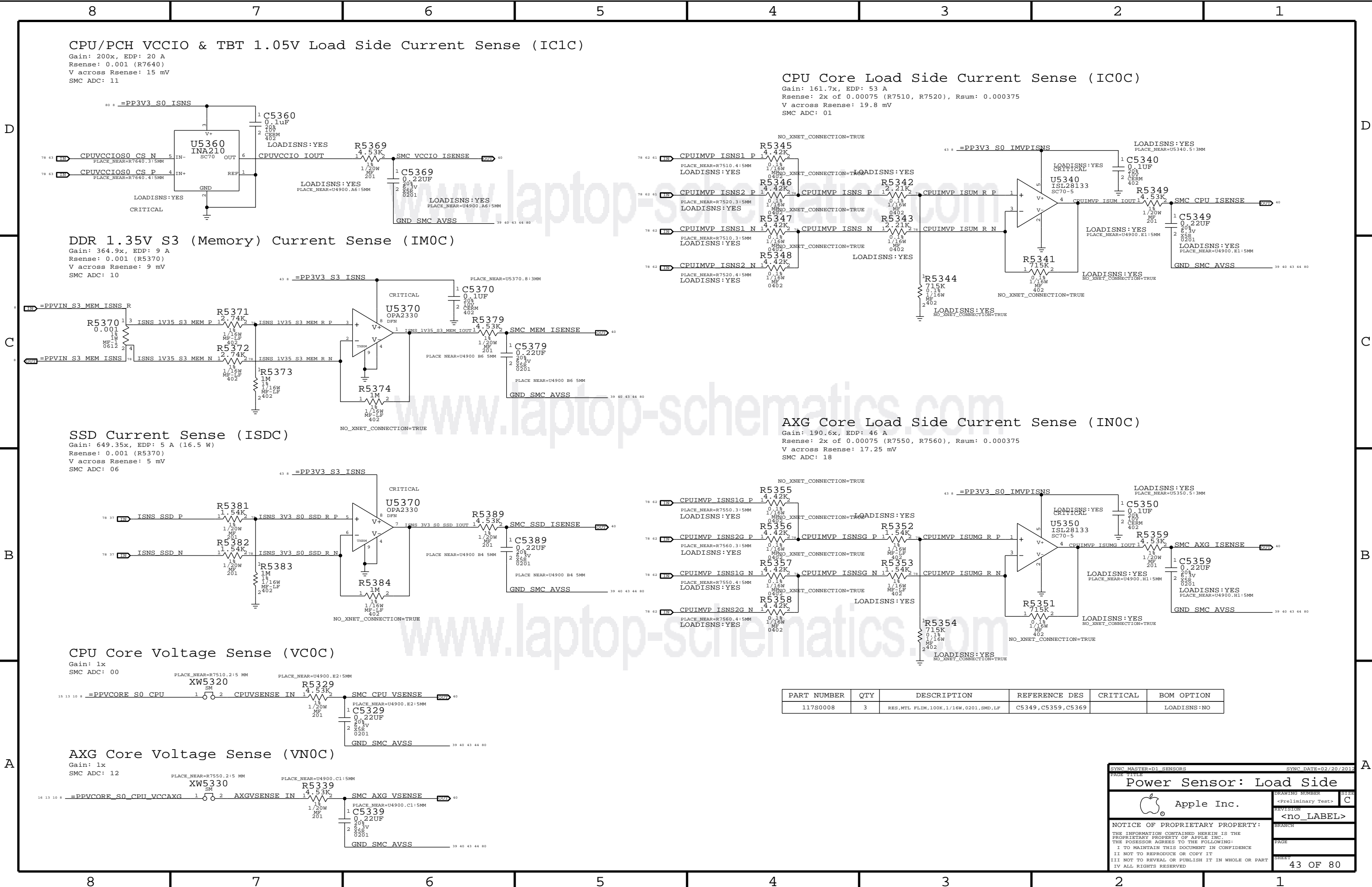
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 8 =PP5V_S0_LPCPLUS
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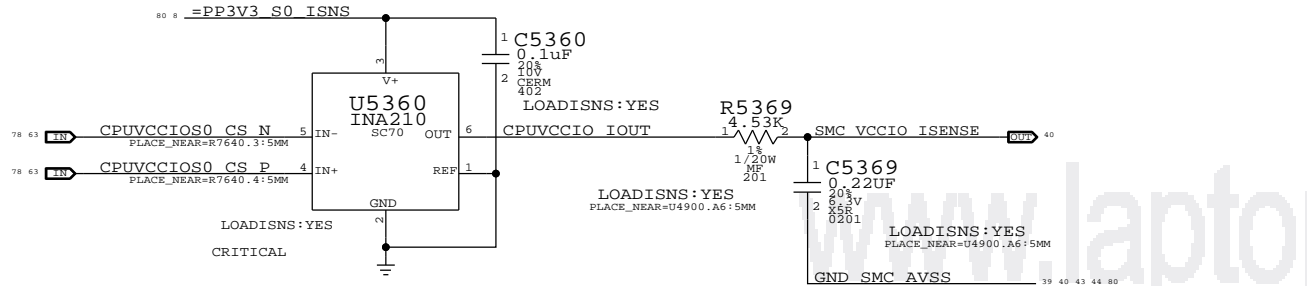


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PAGE TITLE		PAGE	
SMBus Connections		DRAWING NUMBER	SIZE
Apple Inc.		<Preliminary Test>	C
REVISION		<no_LABEL>	
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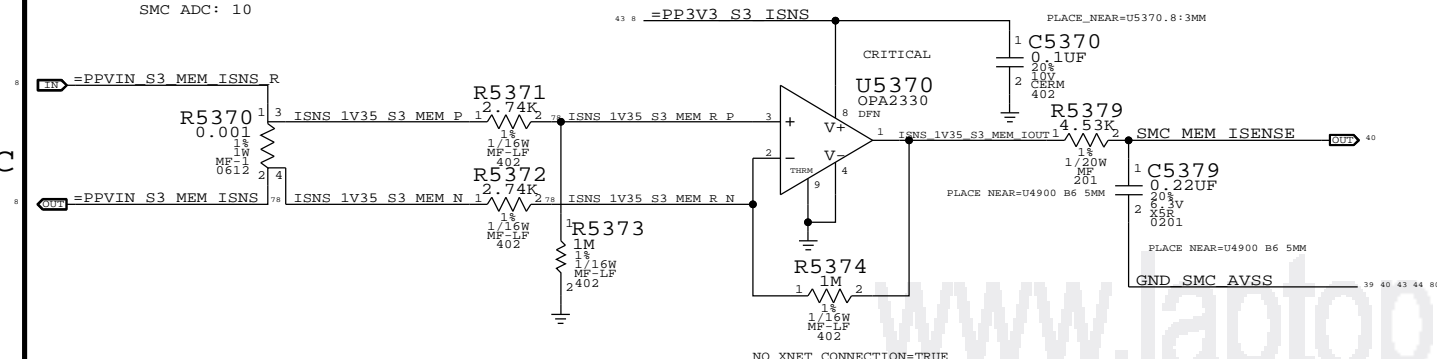
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 15 mV
SMC ADC: 11



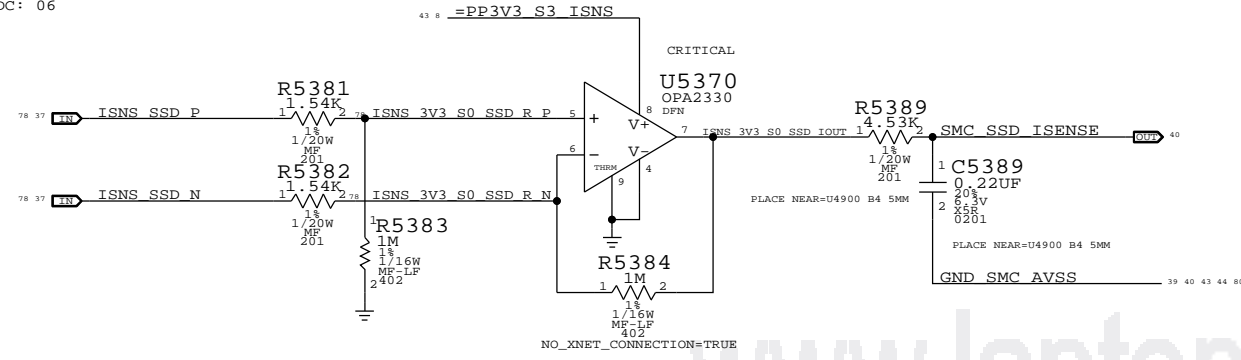
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
SMC ADC: 10



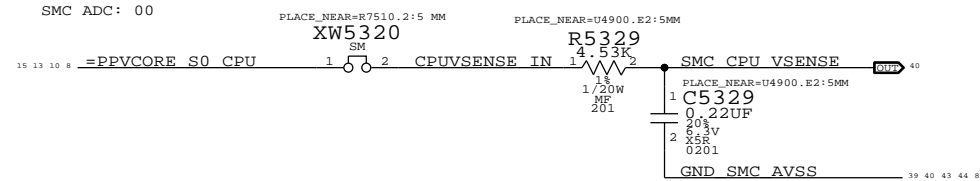
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
Rsense: 0.001 (R5370)
V across Rsense: 5 mV
SMC ADC: 06



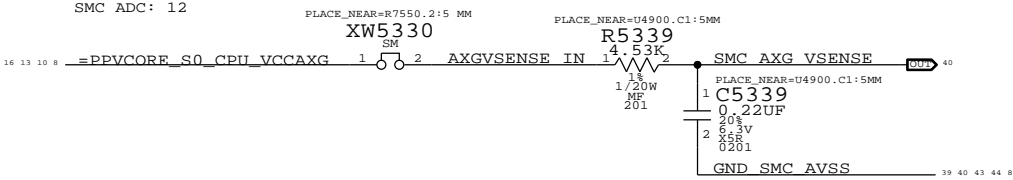
CPU Core Voltage Sense (VC0C)

Gain: 1x
SMC ADC: 00



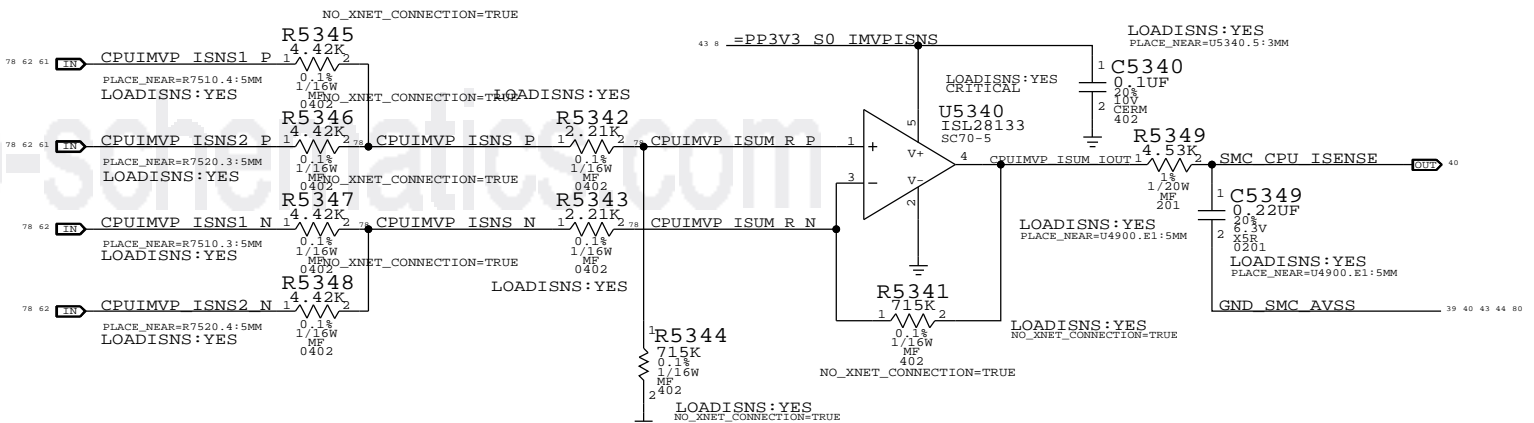
AXG Core Voltage Sense (VN0C)

Gain: 1x
SMC ADC: 12



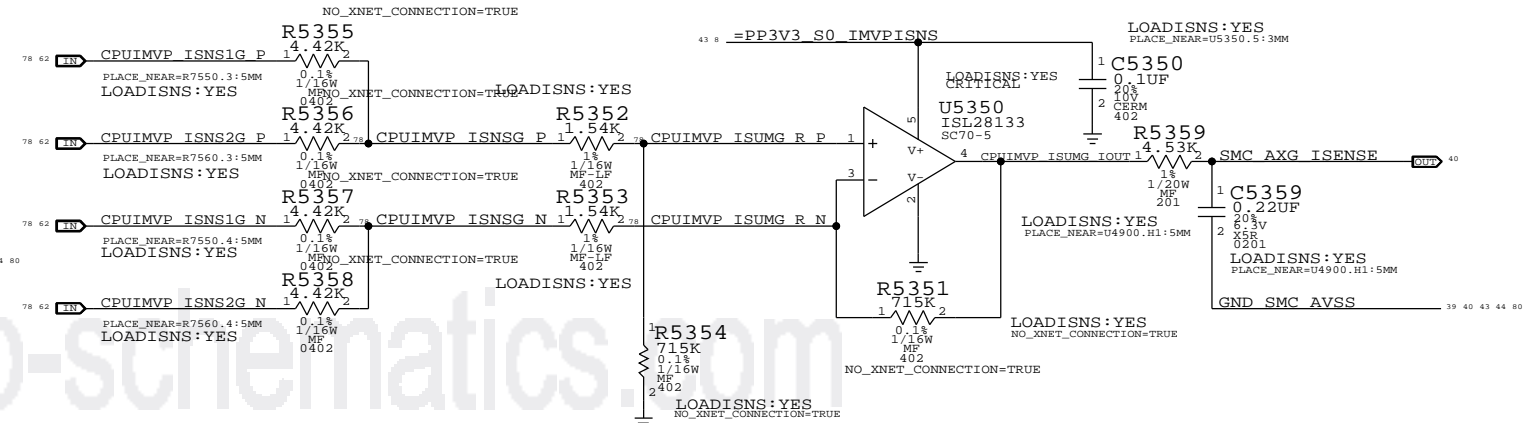
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=D1 SENSORS

SYNC DATE=03/20/2012

Power Sensor: Load Side

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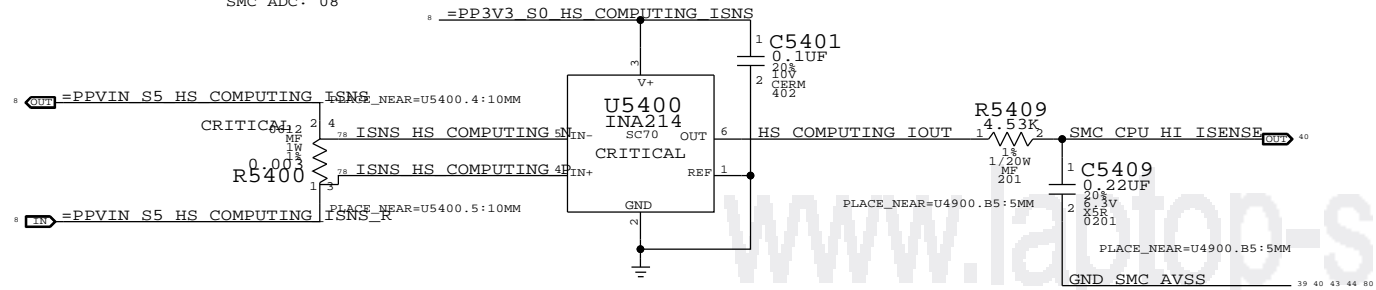
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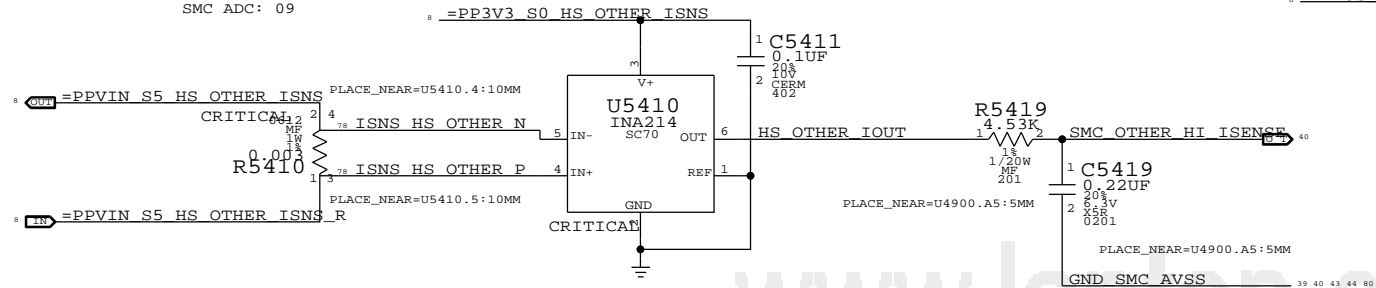
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



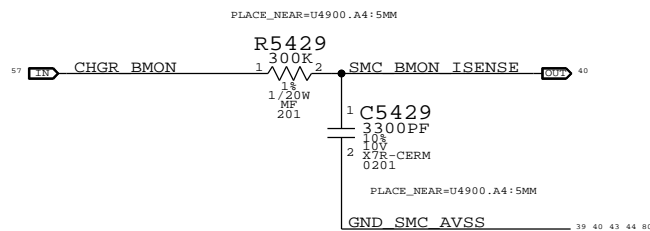
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



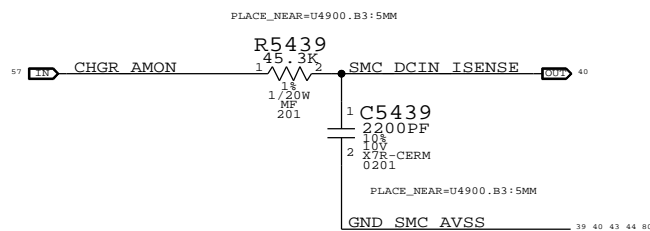
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



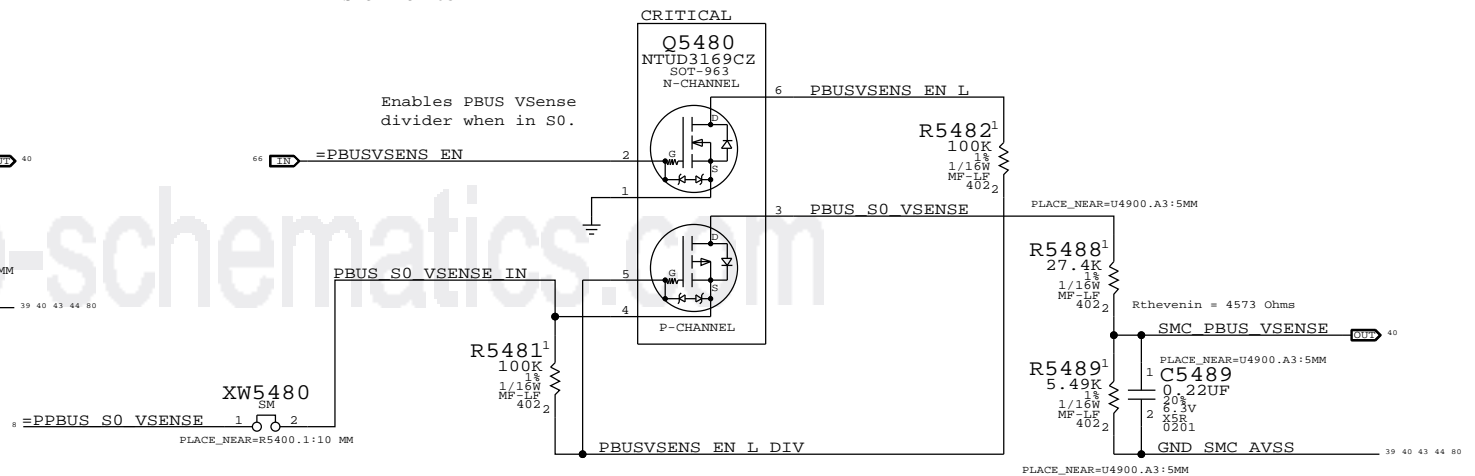
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



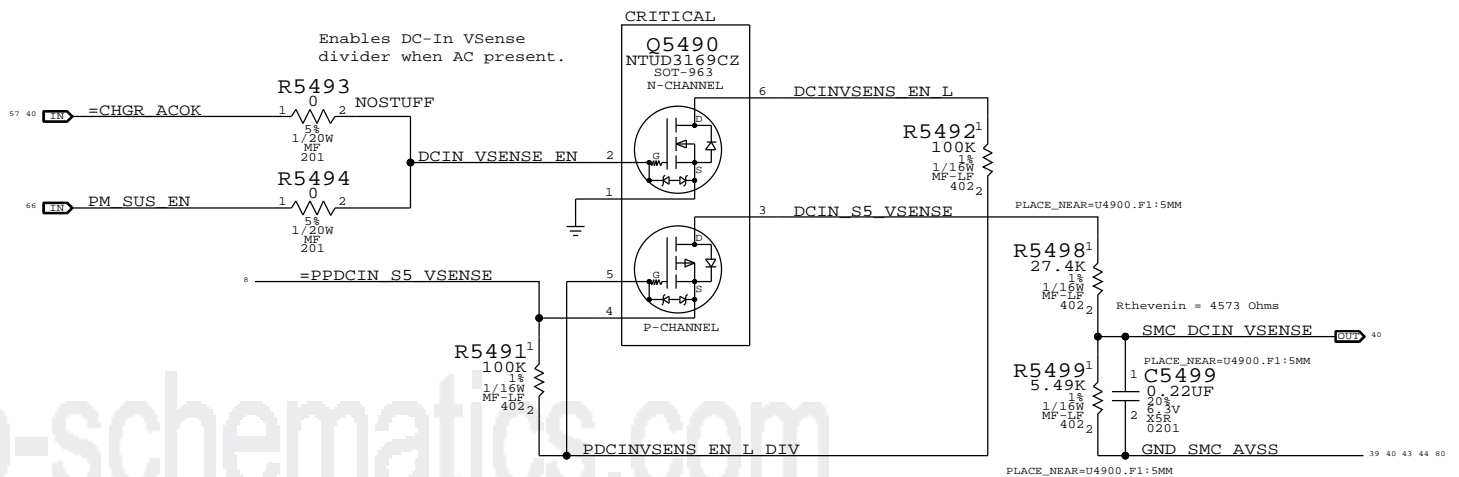
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

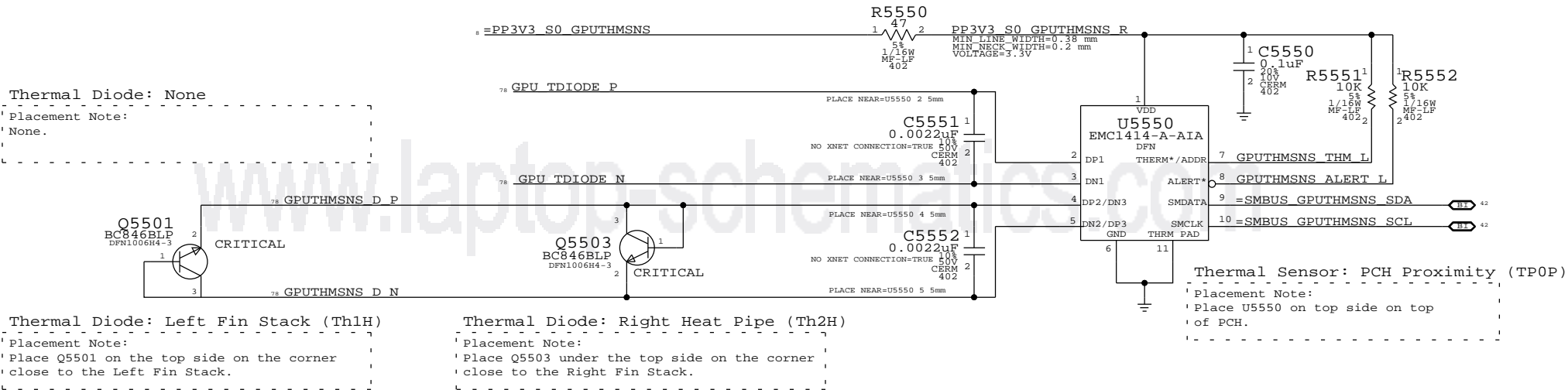
Gain: 0.167x
SMC ADC: 03



SYNC MASTER=D1 SENSORS		SYNC DATE=02/20/2012	
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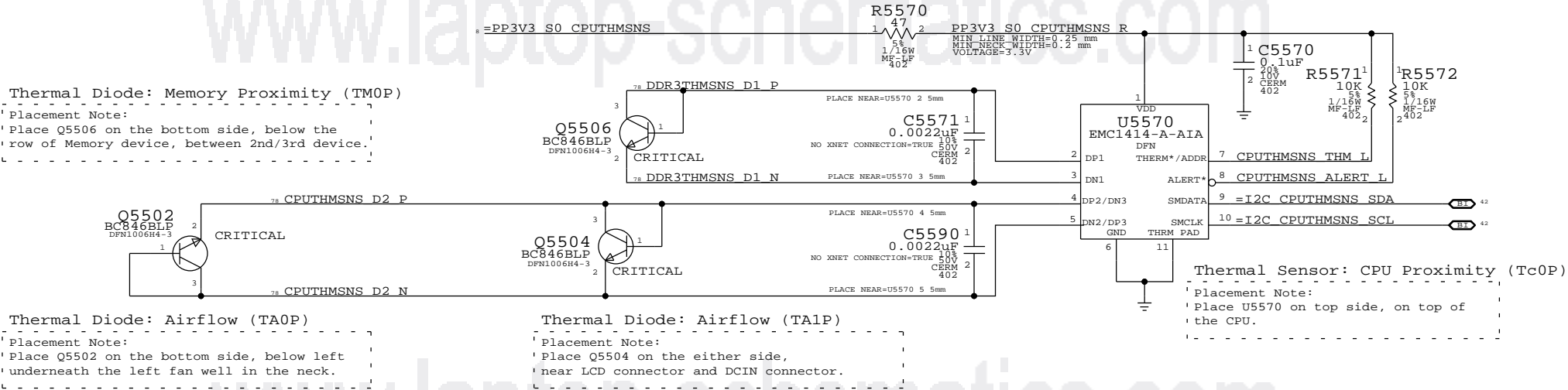
Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99

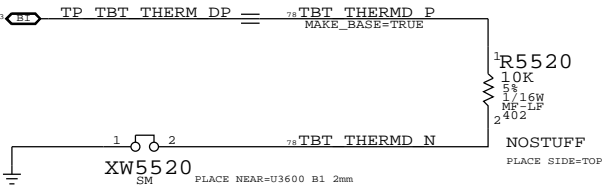


Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

I2C Write: 0x98, I2C Read: 0x99

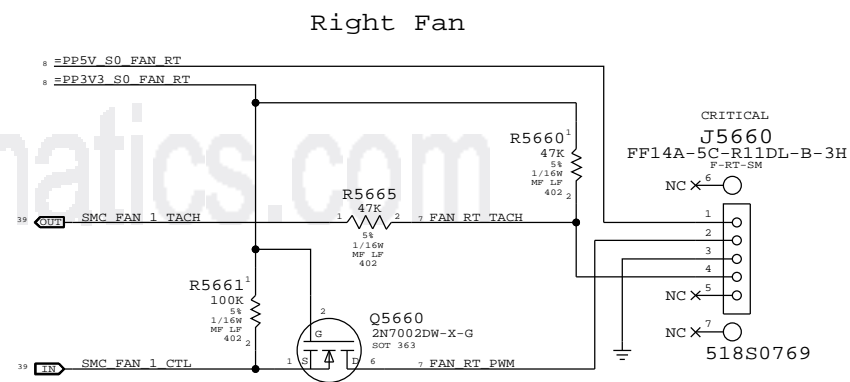
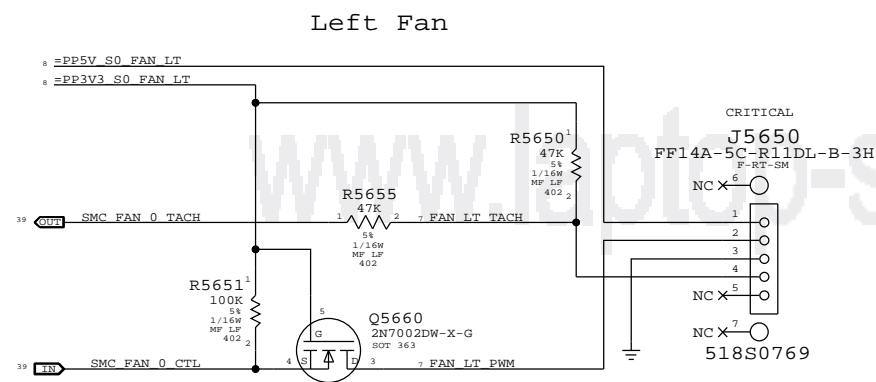



Thermal Sensor: T29 Die



SYNC MASTER=D1 SENSORS		SYNC DATE=03/20/2012	
PAGE TITLE		Thermal Sensors	
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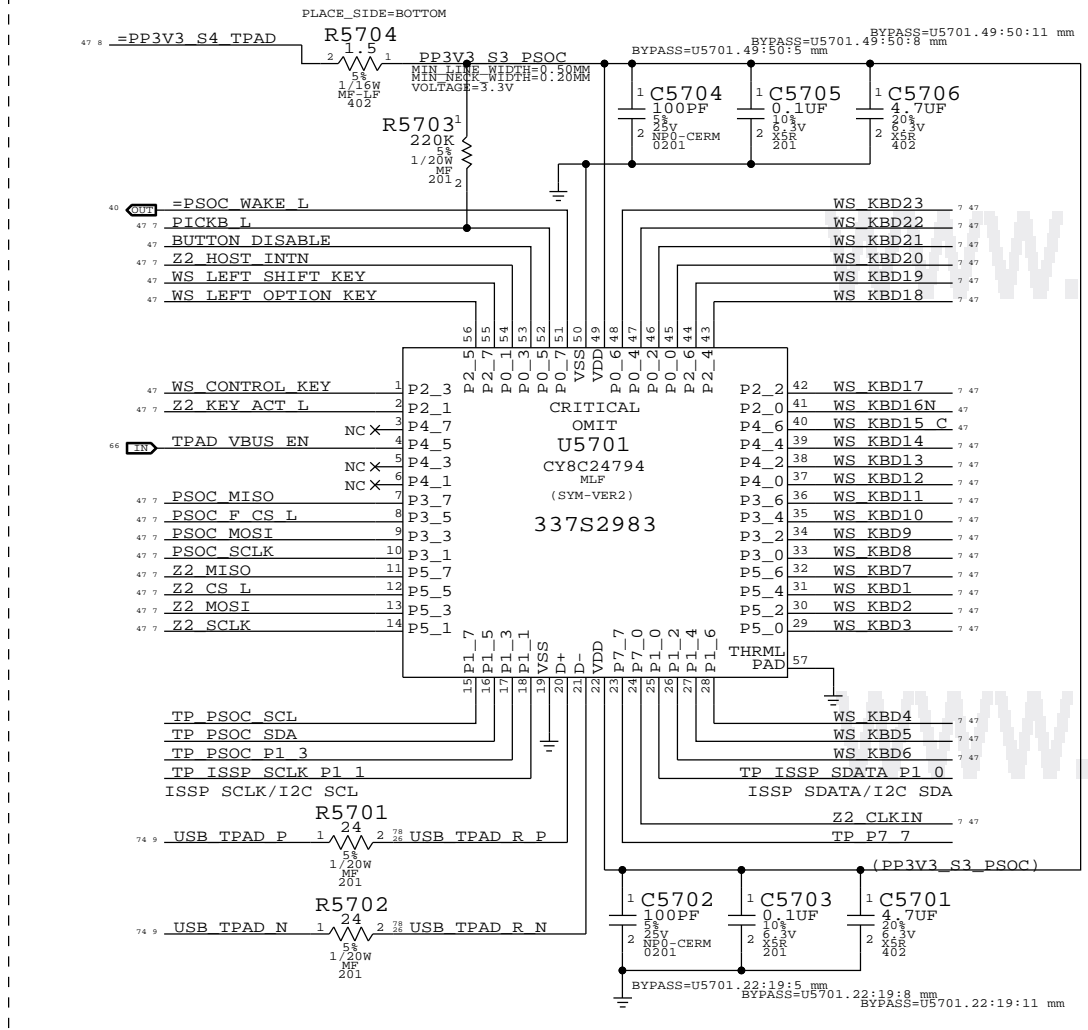
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SYNC MASTER=J5 MLB		SYNC DATE=07/29/2011	
PAGE TITLE		Fan Connectors	
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		SHEET	46 OF 80

PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

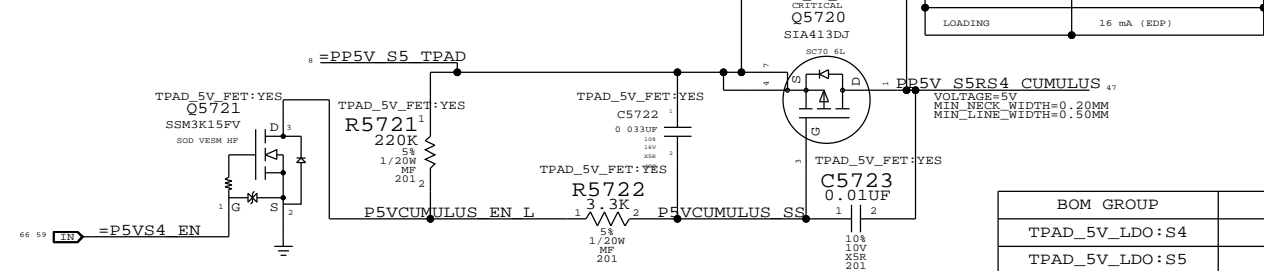


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	VOUT	80UA	0.204 V	16.32E-6 W	
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.72E-3 W	
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	VDD	14MA (MAX)	0.021 V	294E-6 W	
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

BOM Options available to CSA 5
TPAD_5V:S4 Original implementation off PP5V_S4
TPAD_5V:LDO_S4 PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5 PP5V_S5 LDO power

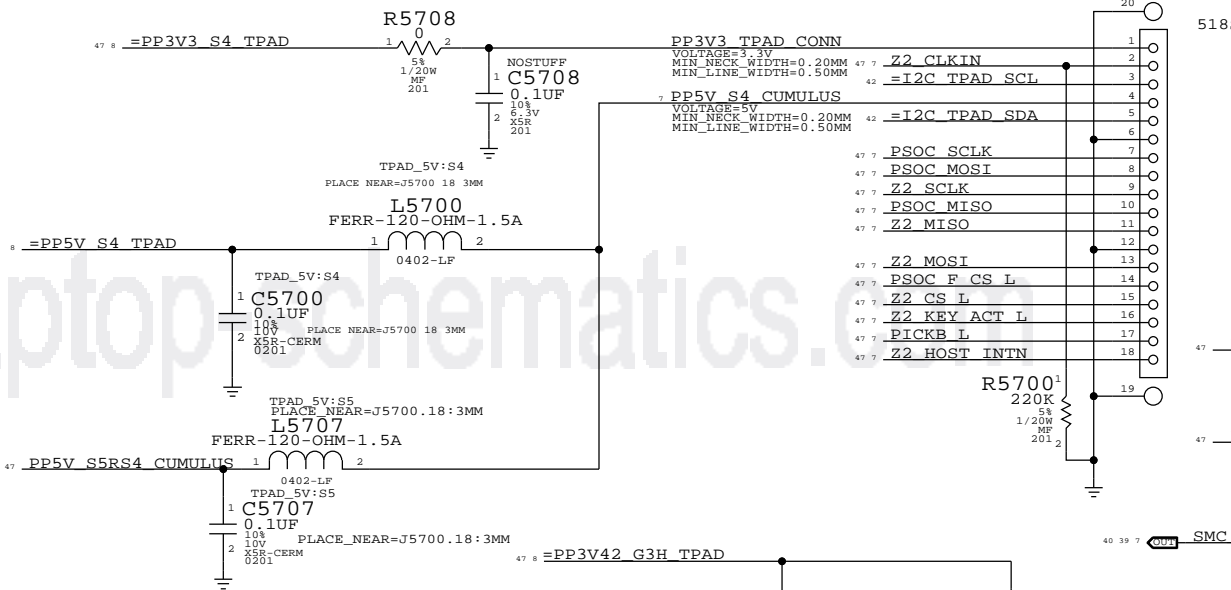
All RC values are TBD

5V TRACKPAD S4 FET



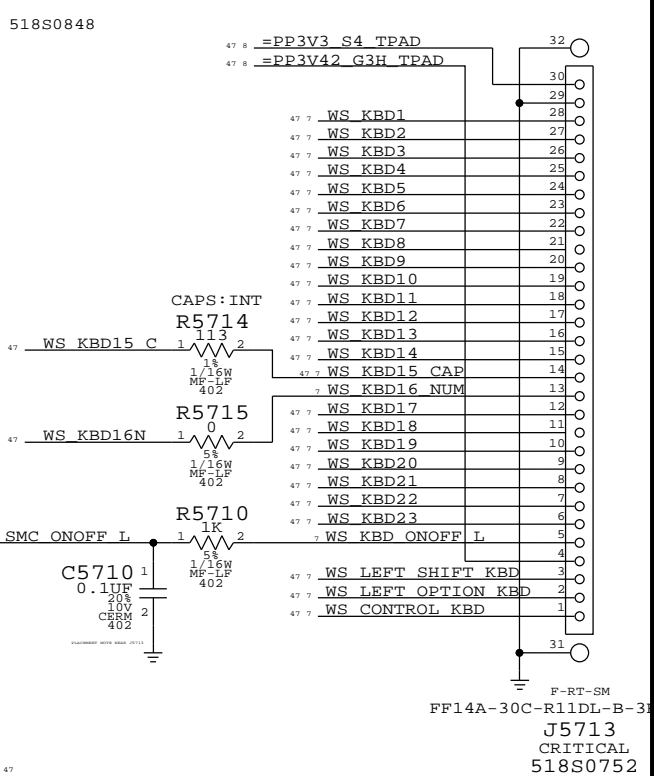
BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES, TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO, TPAD_5V:S5

IPD Flex Connector



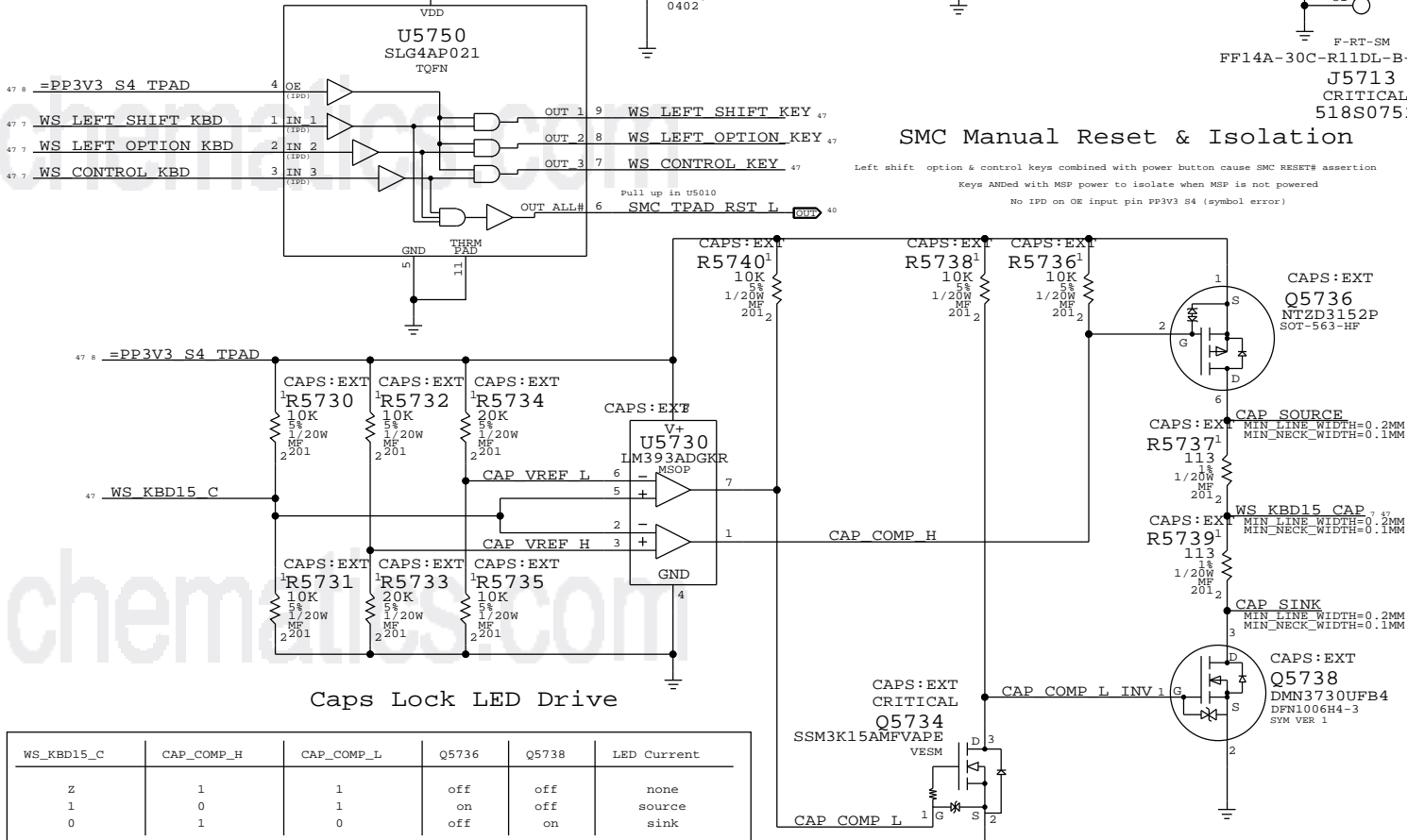
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Keyboard Connector



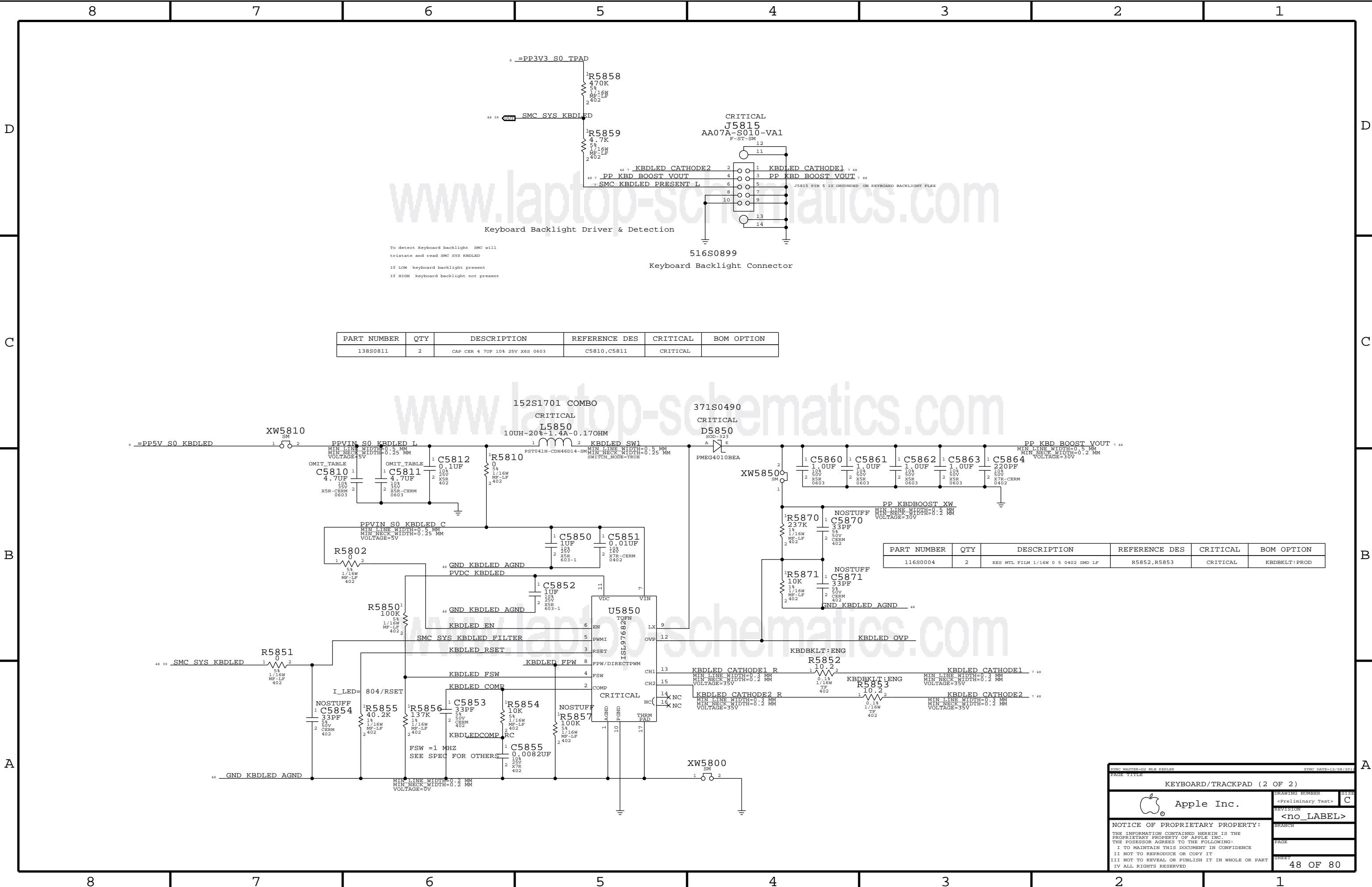
SMC Manual Reset & Isolation

Left shift option & control keys combined with power button cause SMC RESET# assertion
Keys ANDED with MSP power to isolate when MSP is not powered
No IPD on OE input pin PP3V3 S4 (symbol error)



WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

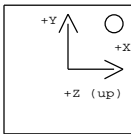
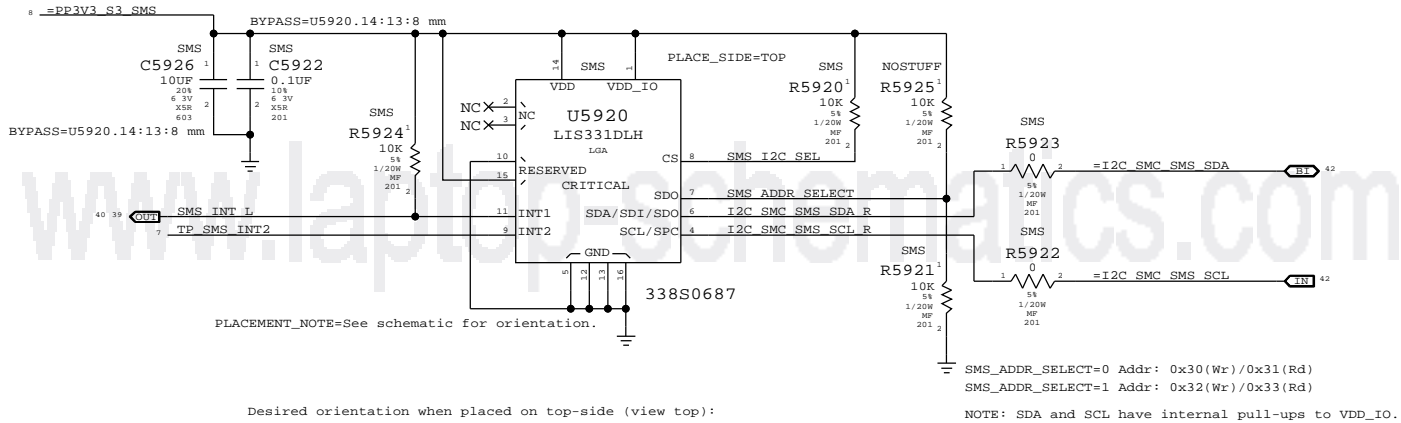
KEYBOARD/TRACKPAD (1 OF 2)	
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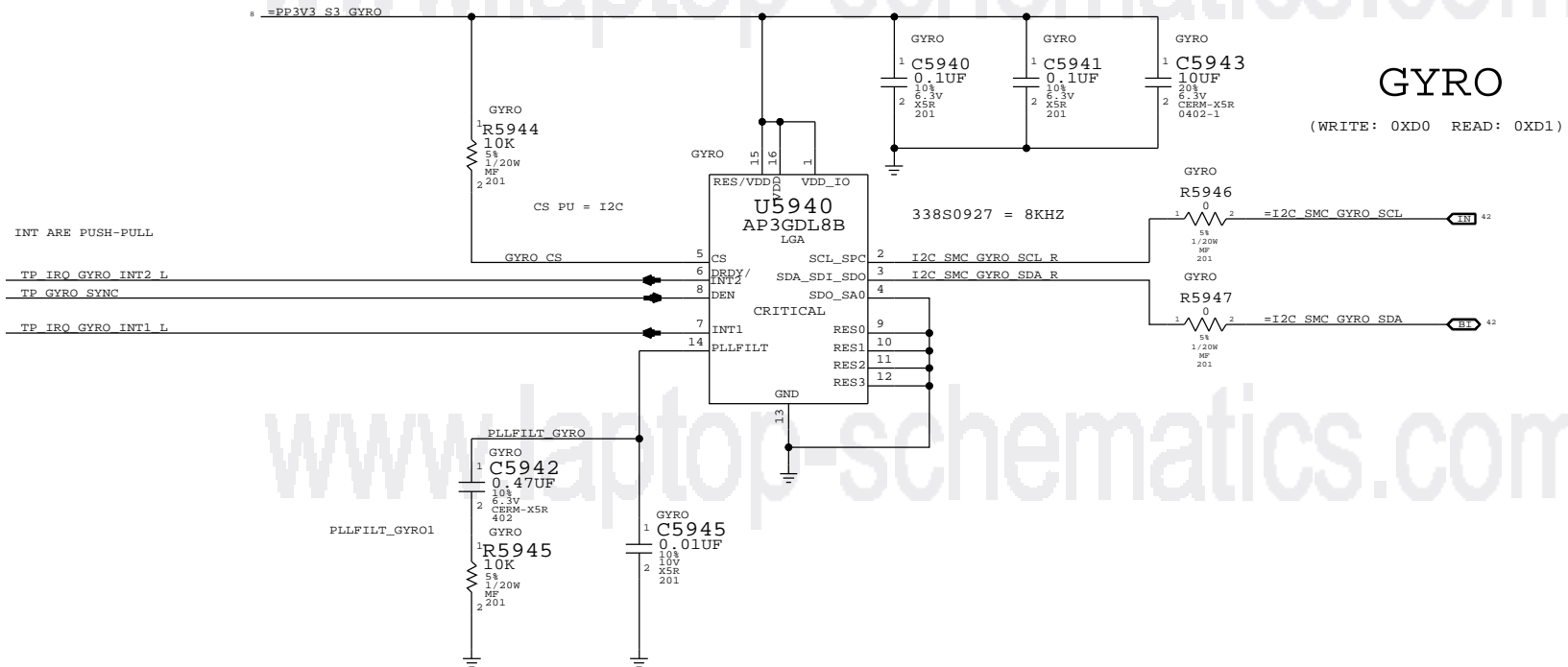
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP CER 4.7UF 10% 25V X6S 0603	C5810,C5811	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES MTL FILM 1/16W 0.5 0402 SMD LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

KEYBOARD/TRACKPAD (2 OF 2)	
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Circle indicates pin 1 location when placed in correct orientation

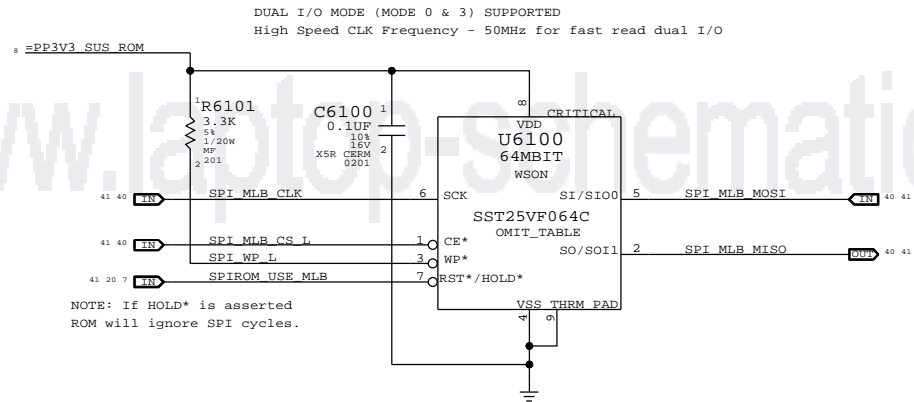



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DRAWING NUMBER		SIZE	
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REVISION		BRANCH	
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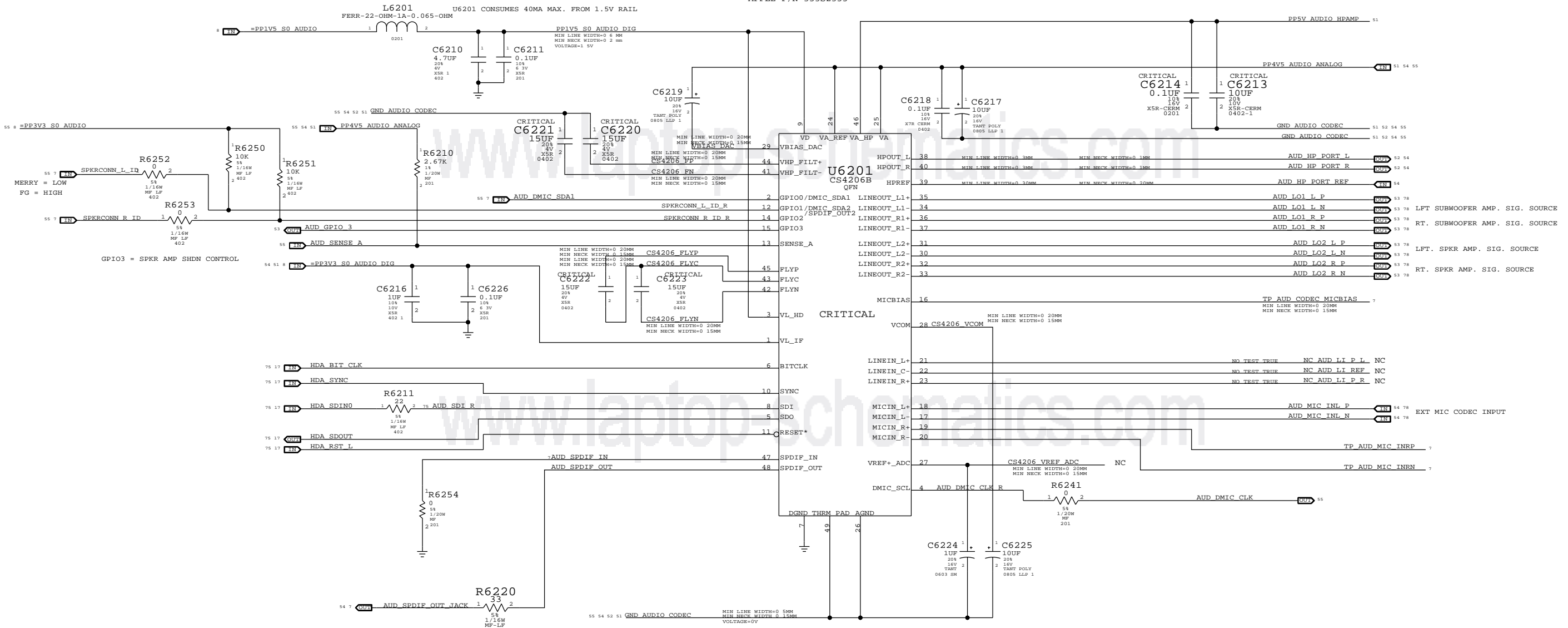
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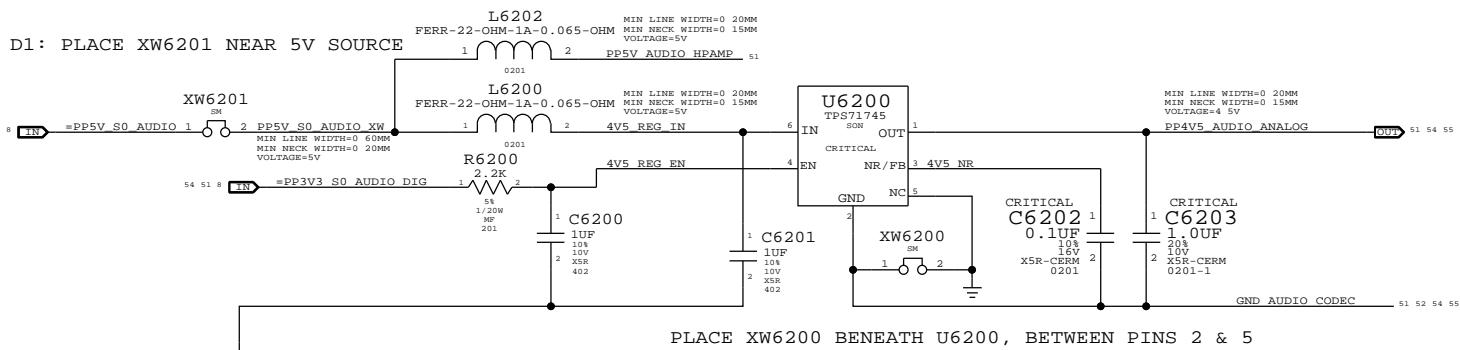


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SPI ROM			
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AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



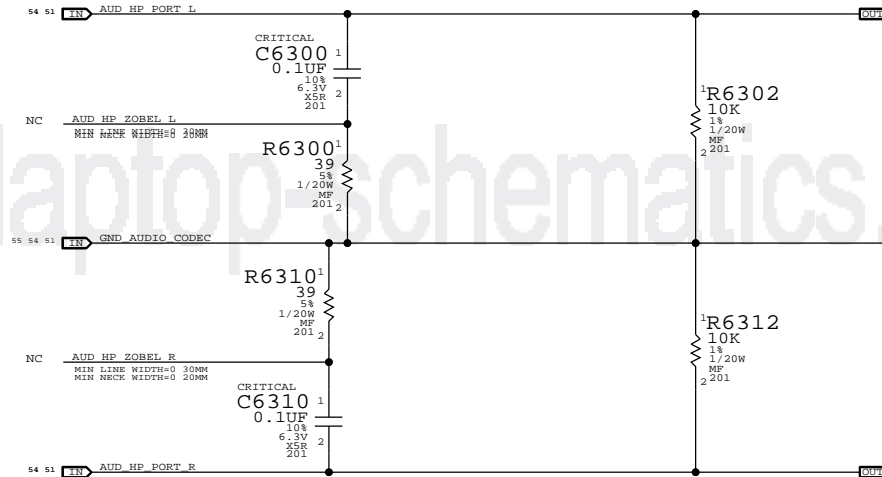
NOTES ON CODEC I/O


DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

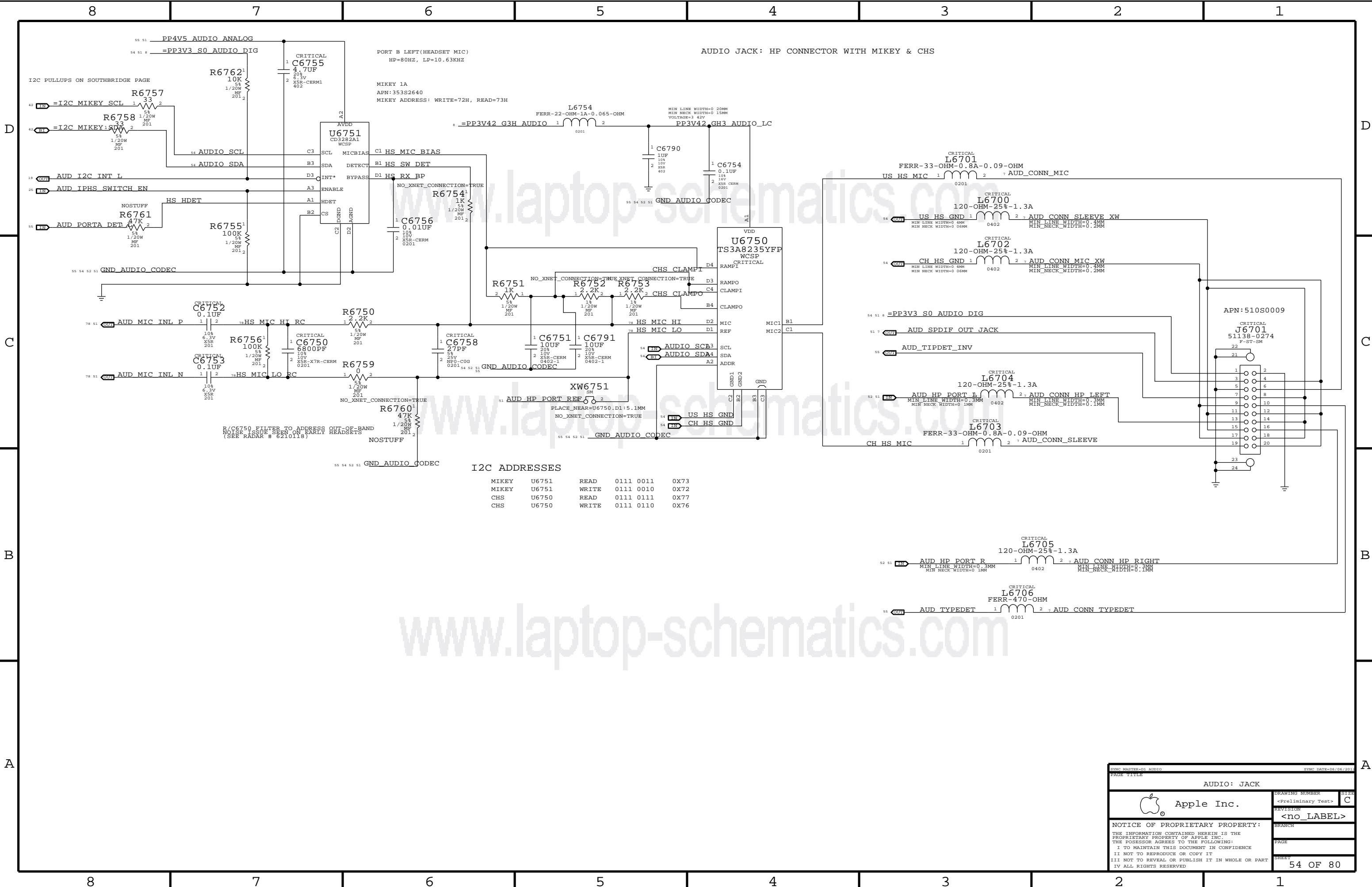
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ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



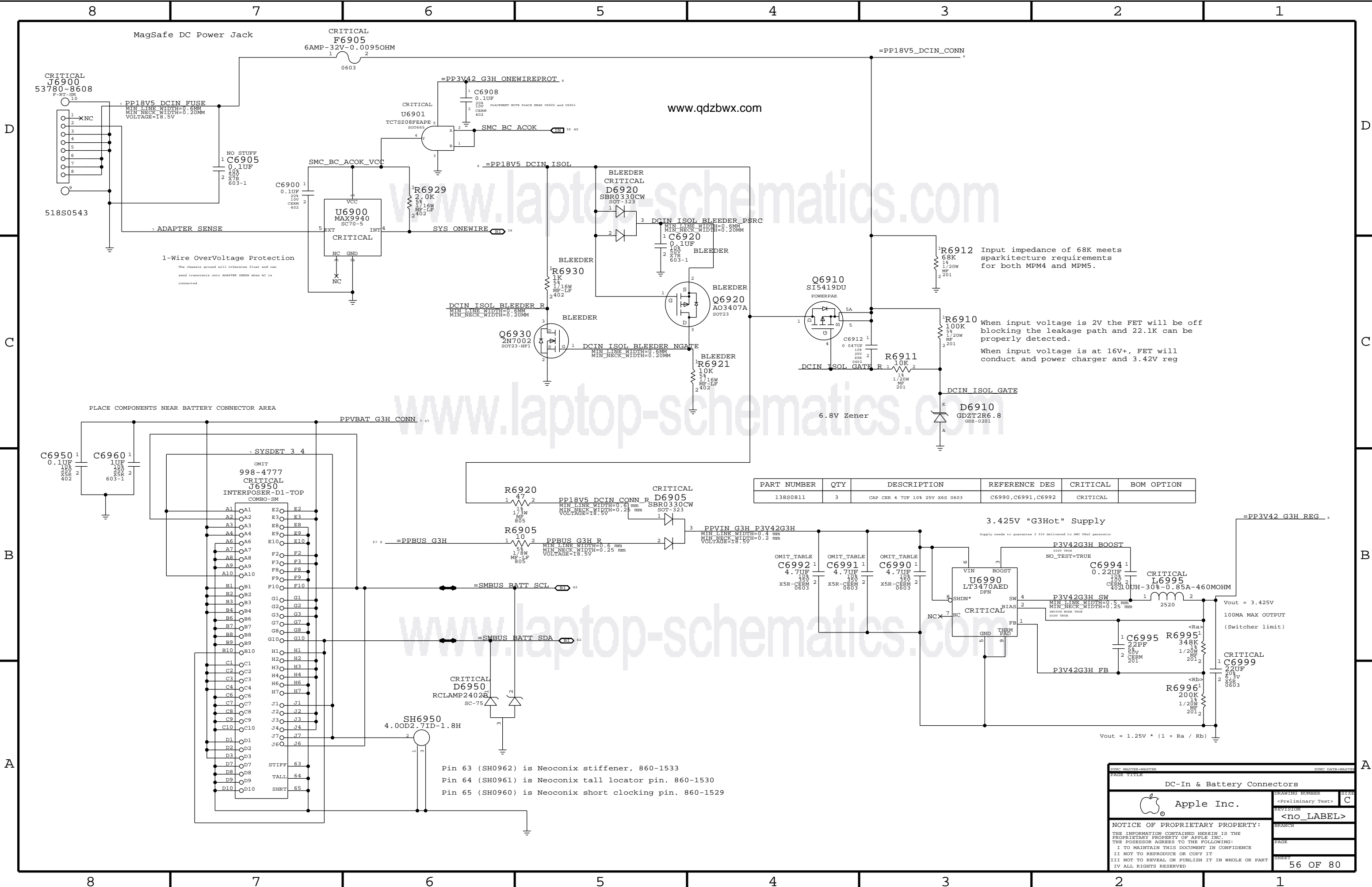
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AUDIO: HEADPHONE FILTER			
	Apple Inc.	DRAWING NUMBER	SIZE
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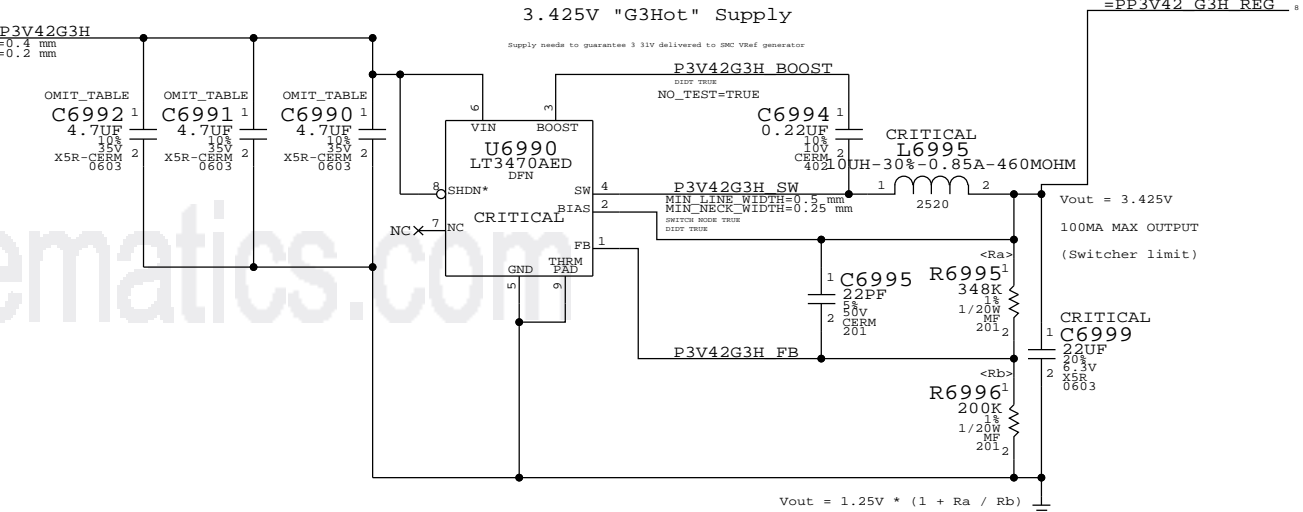
I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

AUDIO: JACK		DRAWING NUMBER	SIZE
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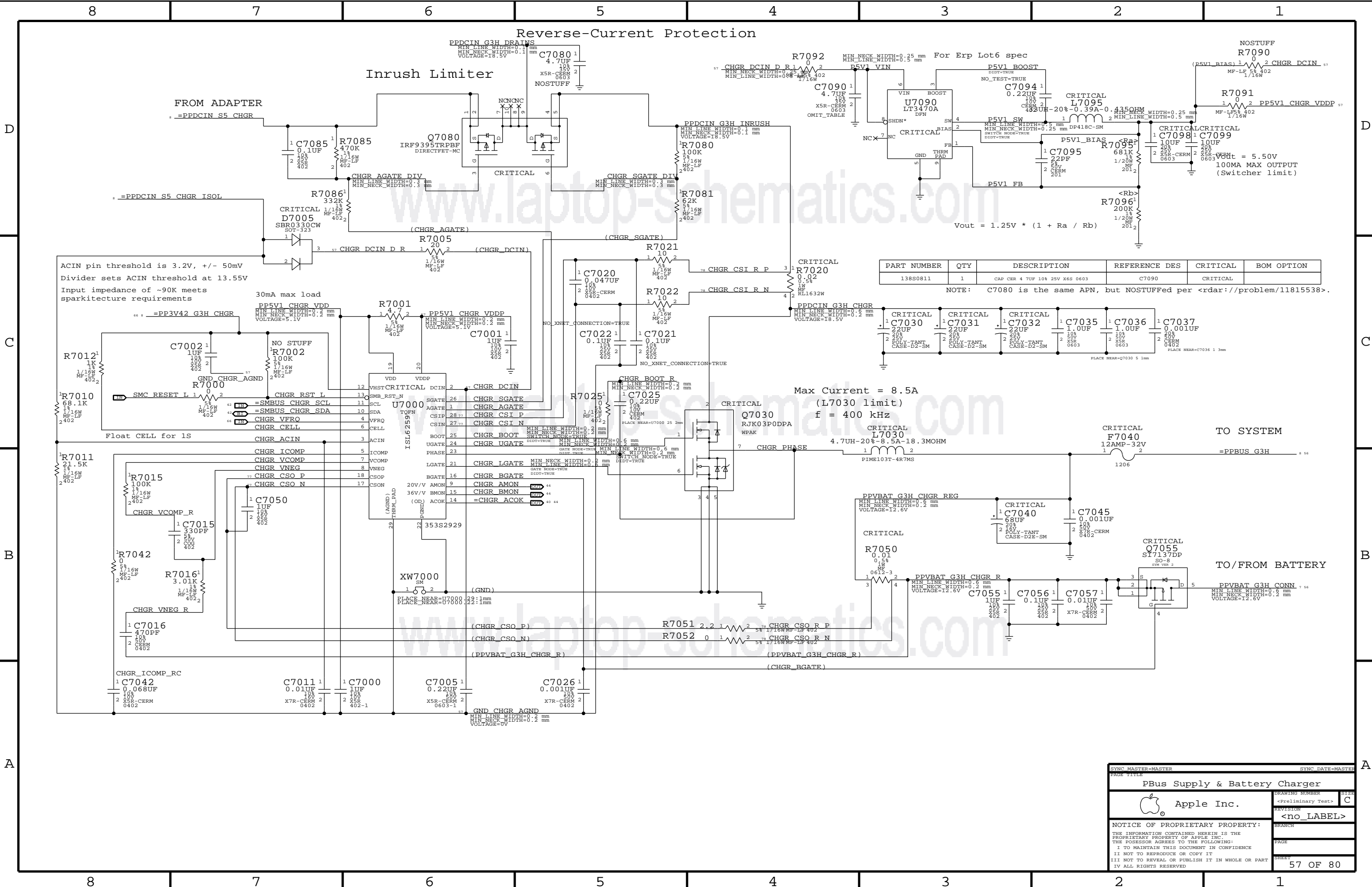


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP CER 4 7UF 10% 25V X6S 0603	C6990,C6991,C6992	CRITICAL	




Pin 63 (SH0962) is Neoconix stiffener, 860-1533
Pin 64 (SH0961) is Neoconix tall locator pin. 860-1530
Pin 65 (SH0960) is Neoconix short clocking pin. 860-1529

PAGE TITLE		PAGE TITLE	
DC-In & Battery Connectors		DC-In & Battery Connectors	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP CER 4 7UF 10% 25V X6S 0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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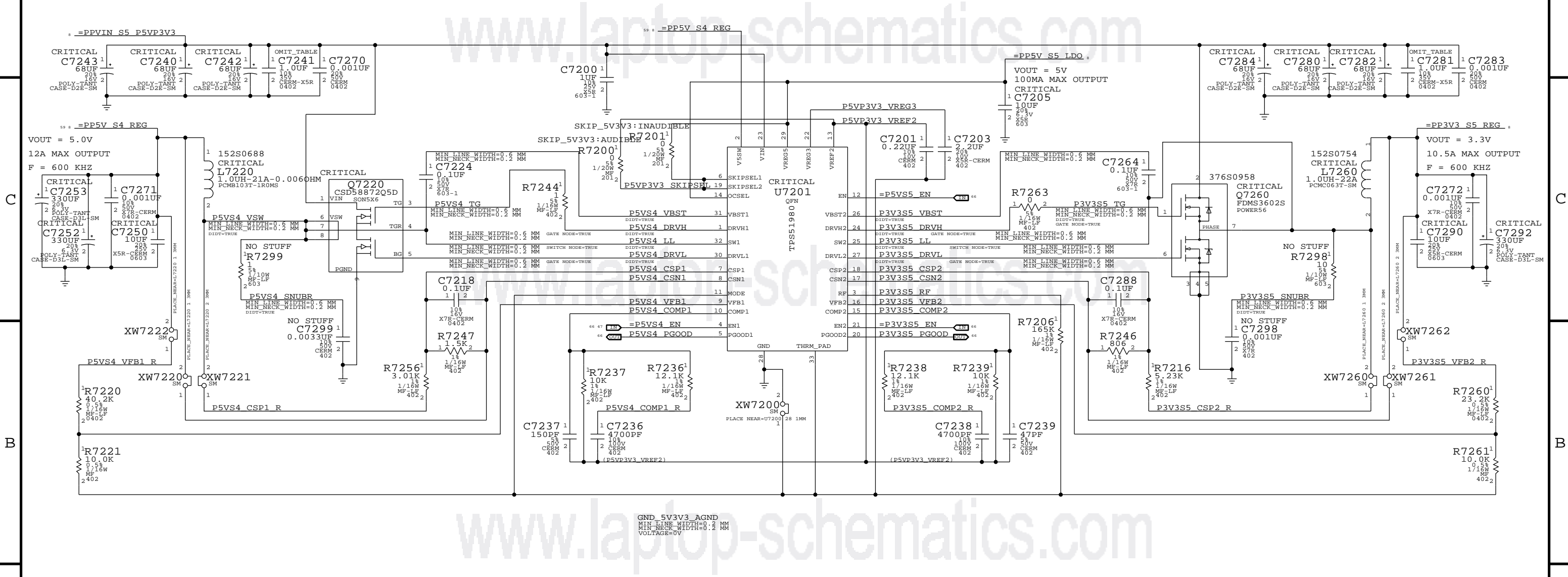
D

C

B

A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7241,C7281	CRITICAL	




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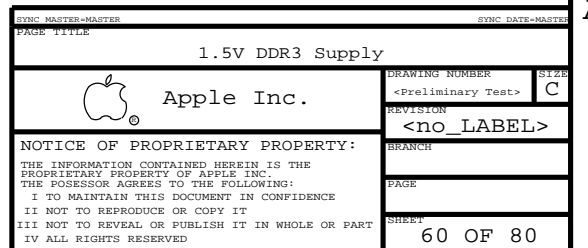
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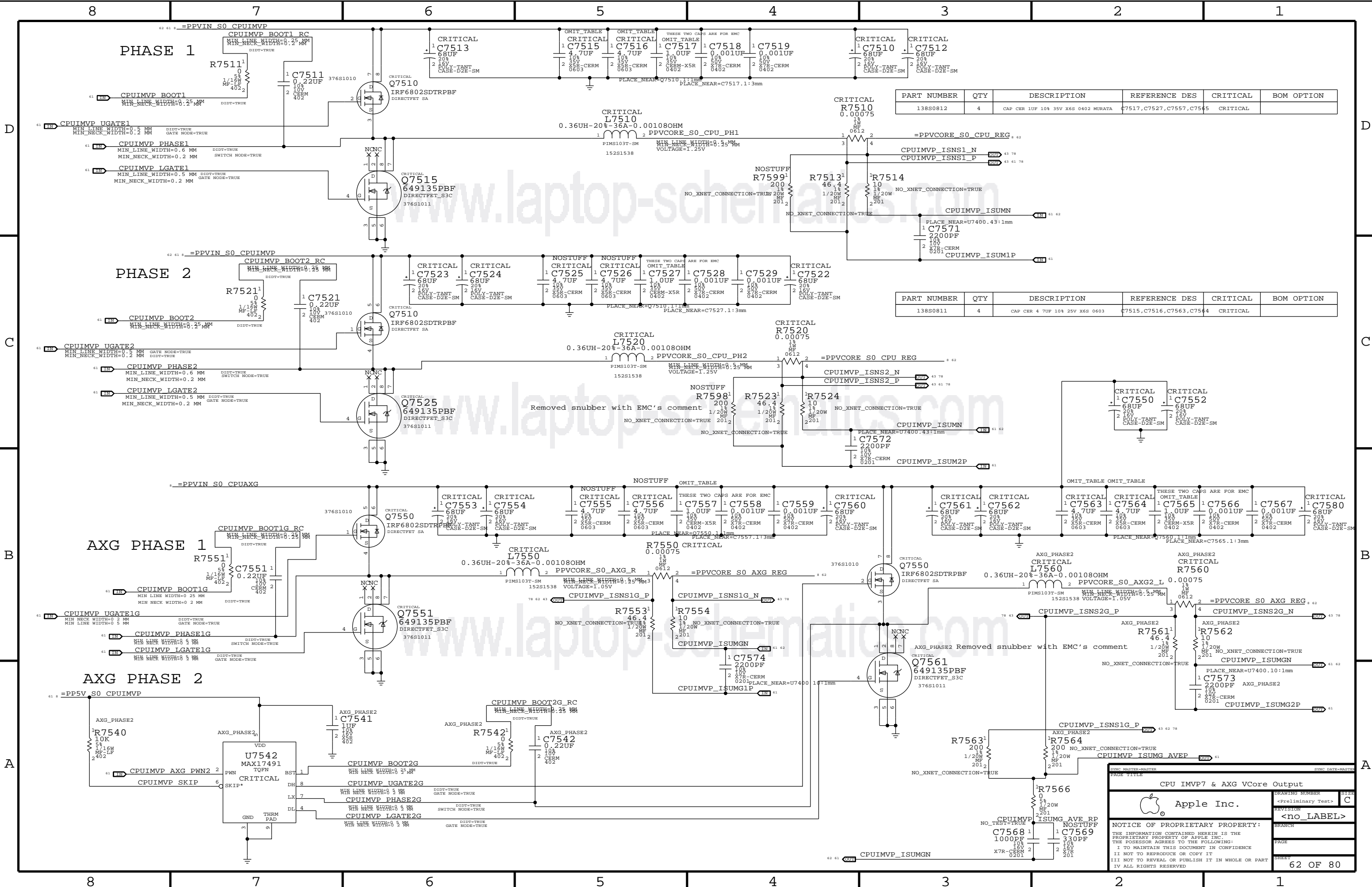
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
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5V / 3.3V Power Supply		Drawing	
 Apple Inc.		DRAWING NUMBER	SIZE
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES MTL FILM 1/16W 100K 1 0402 SMD LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES MTL FILM 1/16W 60 4K 1 0402 SMD LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET N CH 30V 100MA 7 00HM SOT 723 HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES MTL FILM 1/16W 150K 0402 SMD LF	R7319	CRITICAL	PPDDR:1V5







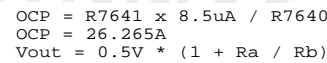
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	4	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7517,C7527,C7557,C7565	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP CER 4 7UF 10% 25V X6S 0603	C7515,C7516,C7563,C7564	CRITICAL	

PAGE TITLE		PAGE NUMBER	
CPU IMVP7 & AXG VCore Output		62 OF 80	
Apple Inc.		DRAWING NUMBER	
		<Preliminary Test>	
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PART NUMBER	QTY	
138S0812	1	CAP CER

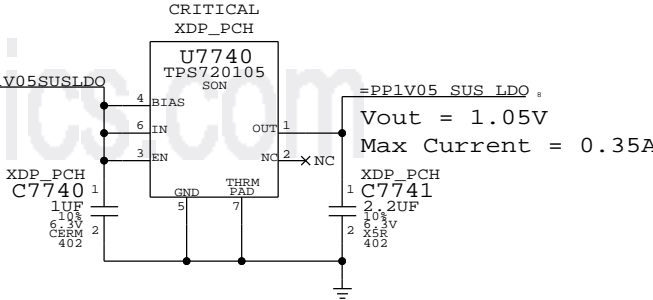
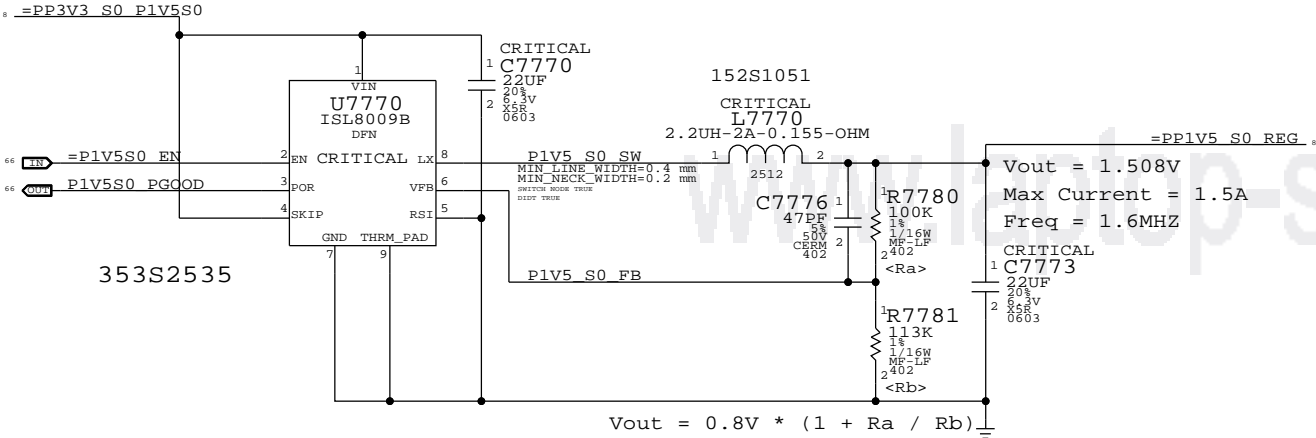
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7624	CRITICAL	



1.5V S0 Switcher

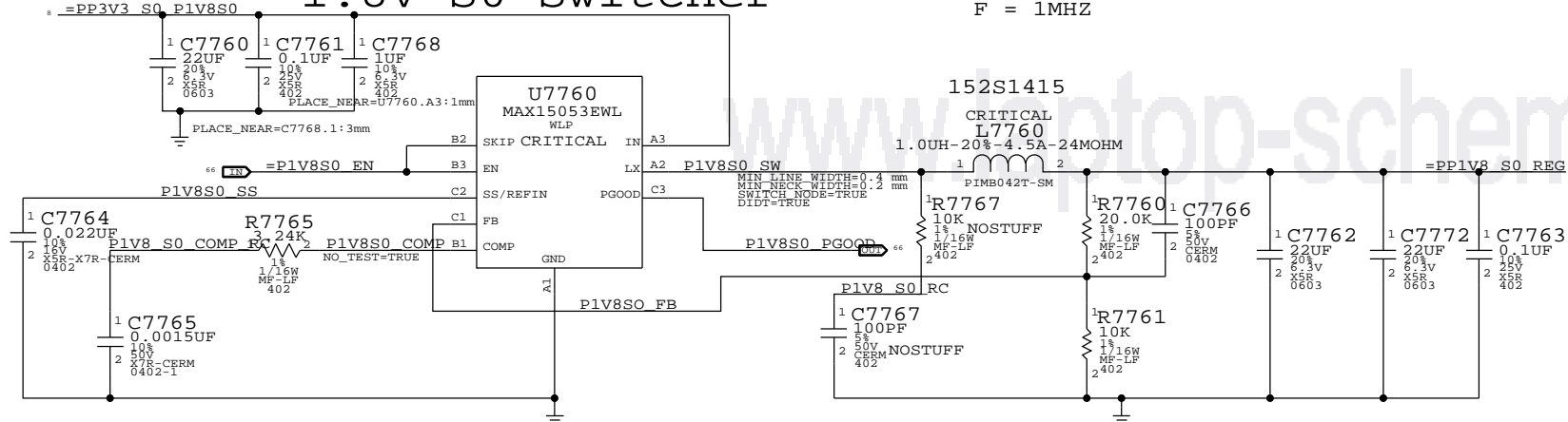
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



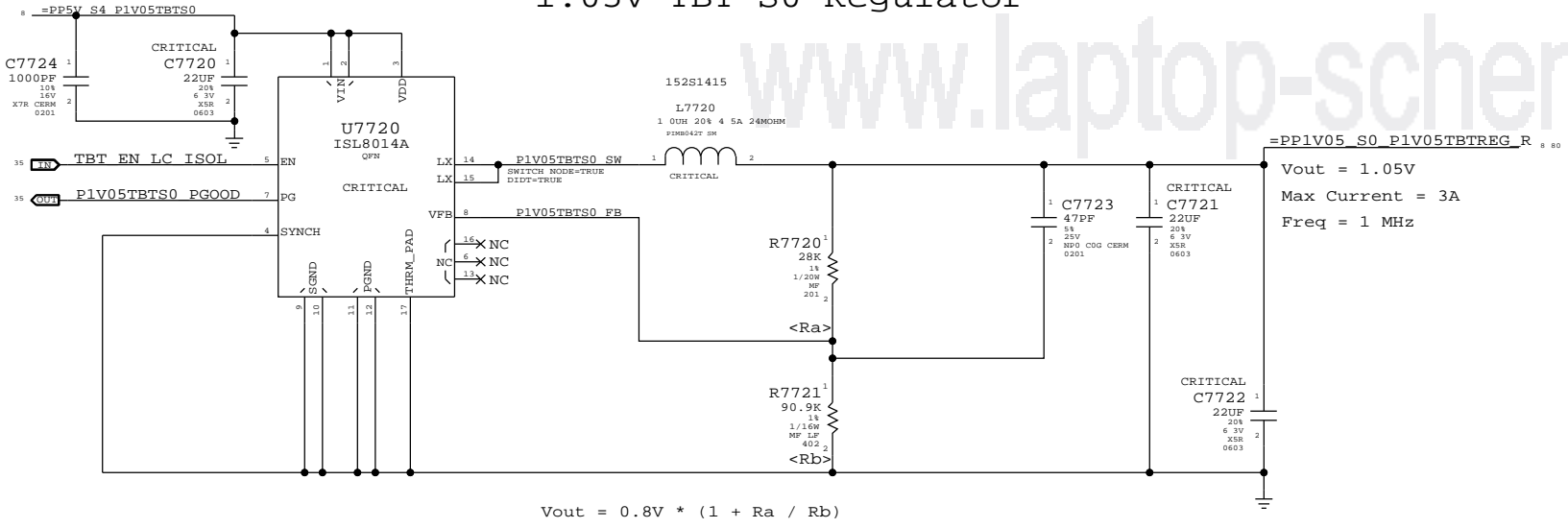
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ

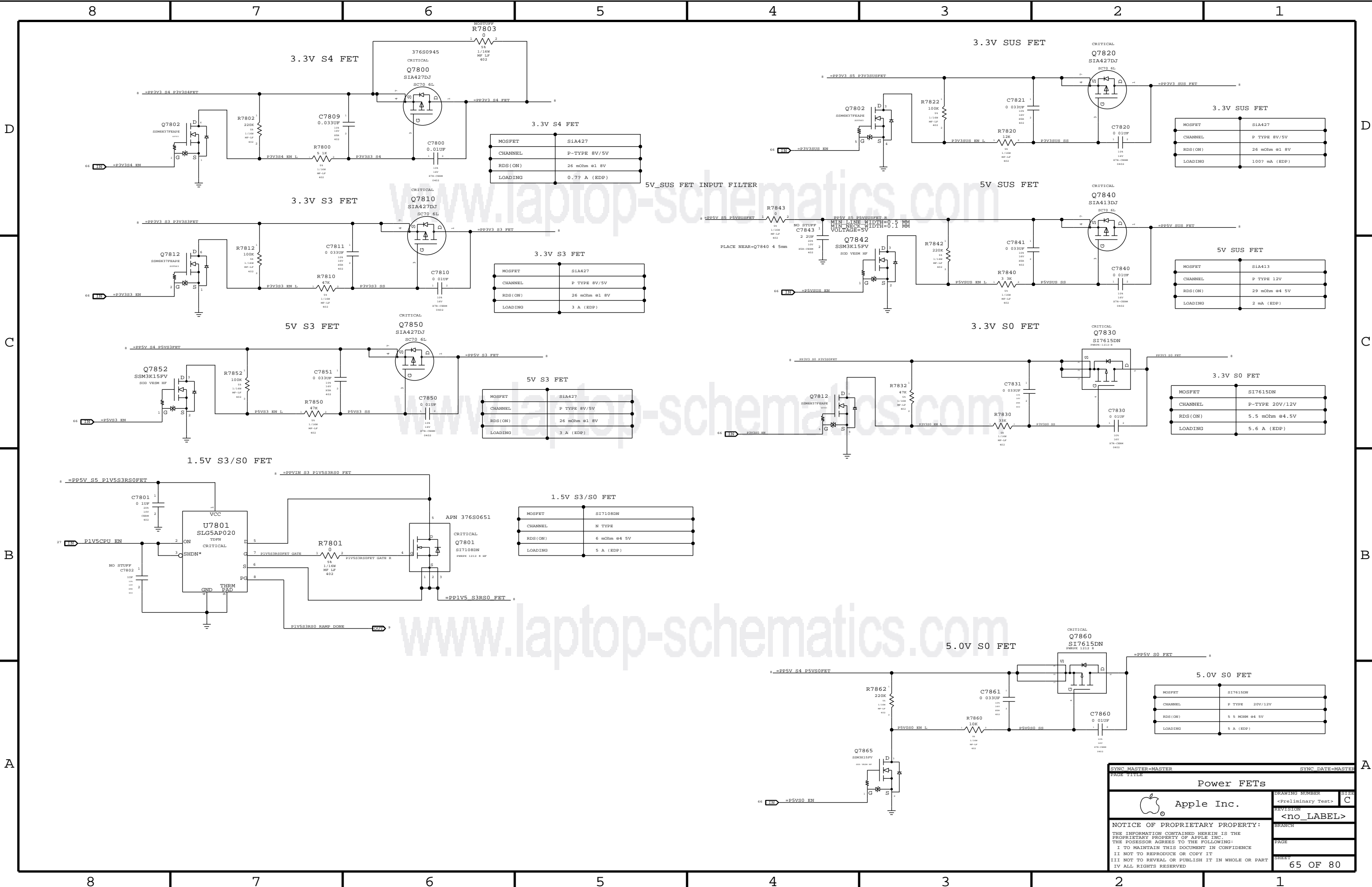


1.05V TBT S0 Regulator

Vout = 1.05V
Max Current = 3A
Freq = 1 MHz



SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE		DRAWING NUMBER	
Misc Power Supplies		C	
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SYNC DATE=MASTER

Power FETs

Apple Inc.

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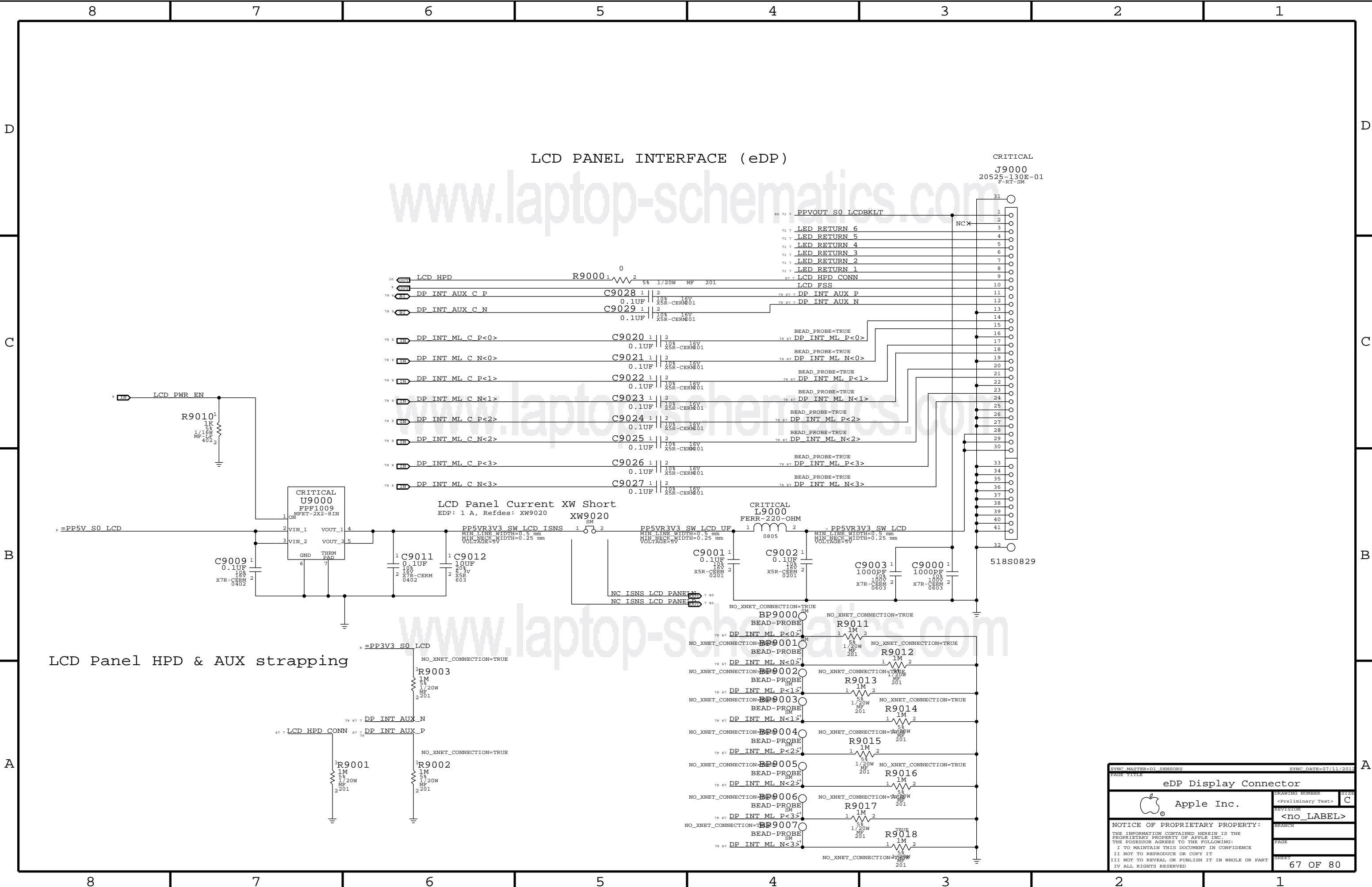
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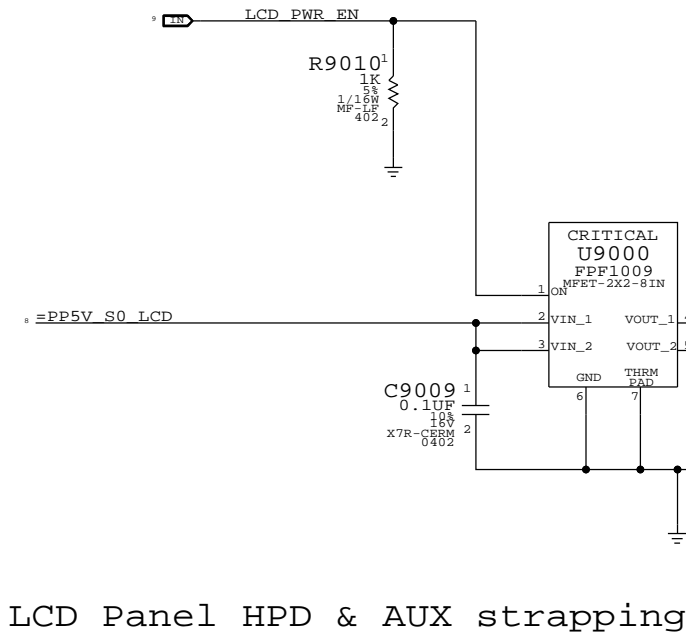
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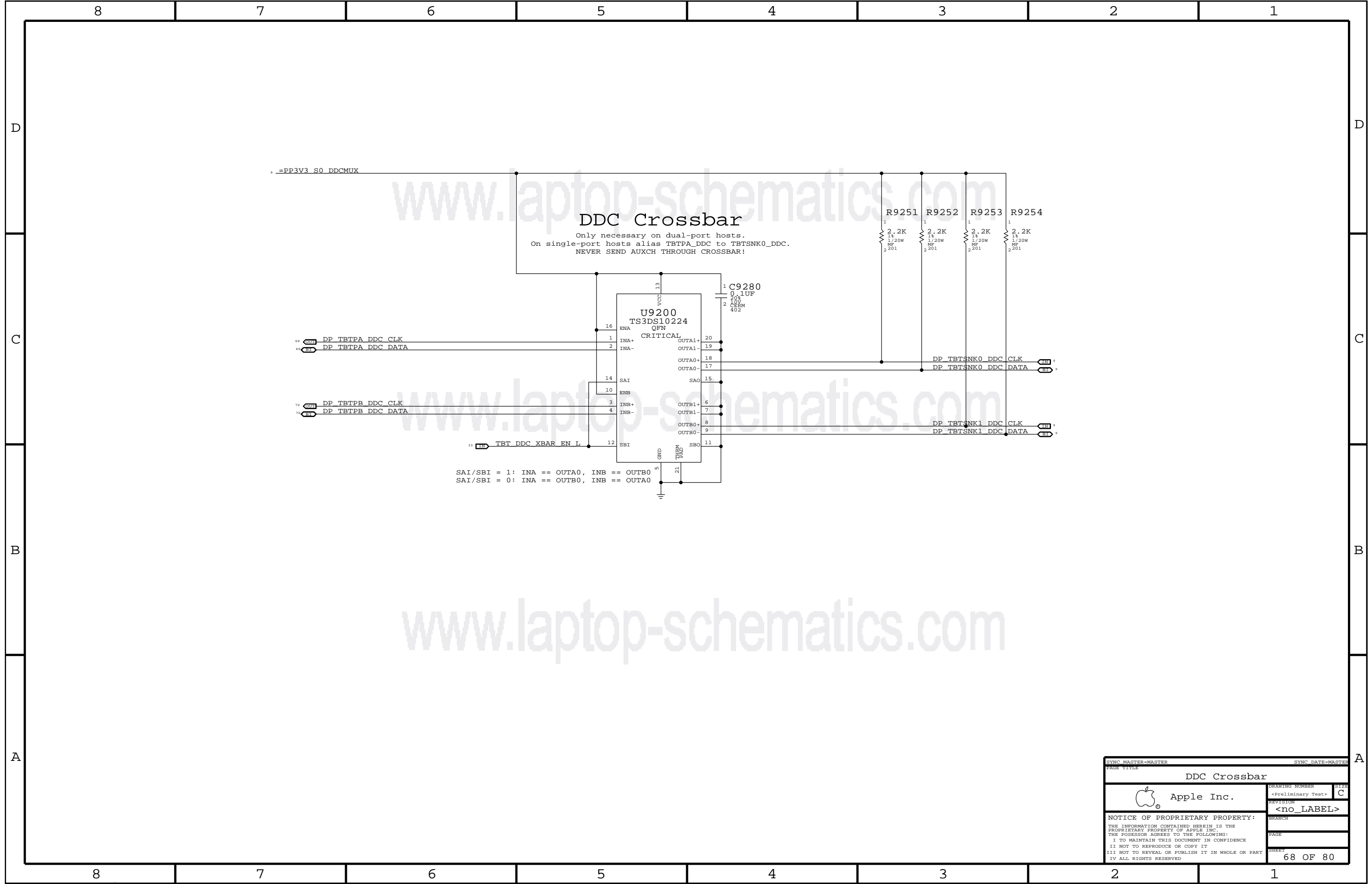
LCD PANEL INTERFACE (eDP)


CRITICAL
J9000
20525-130E-01
F-RT-SM

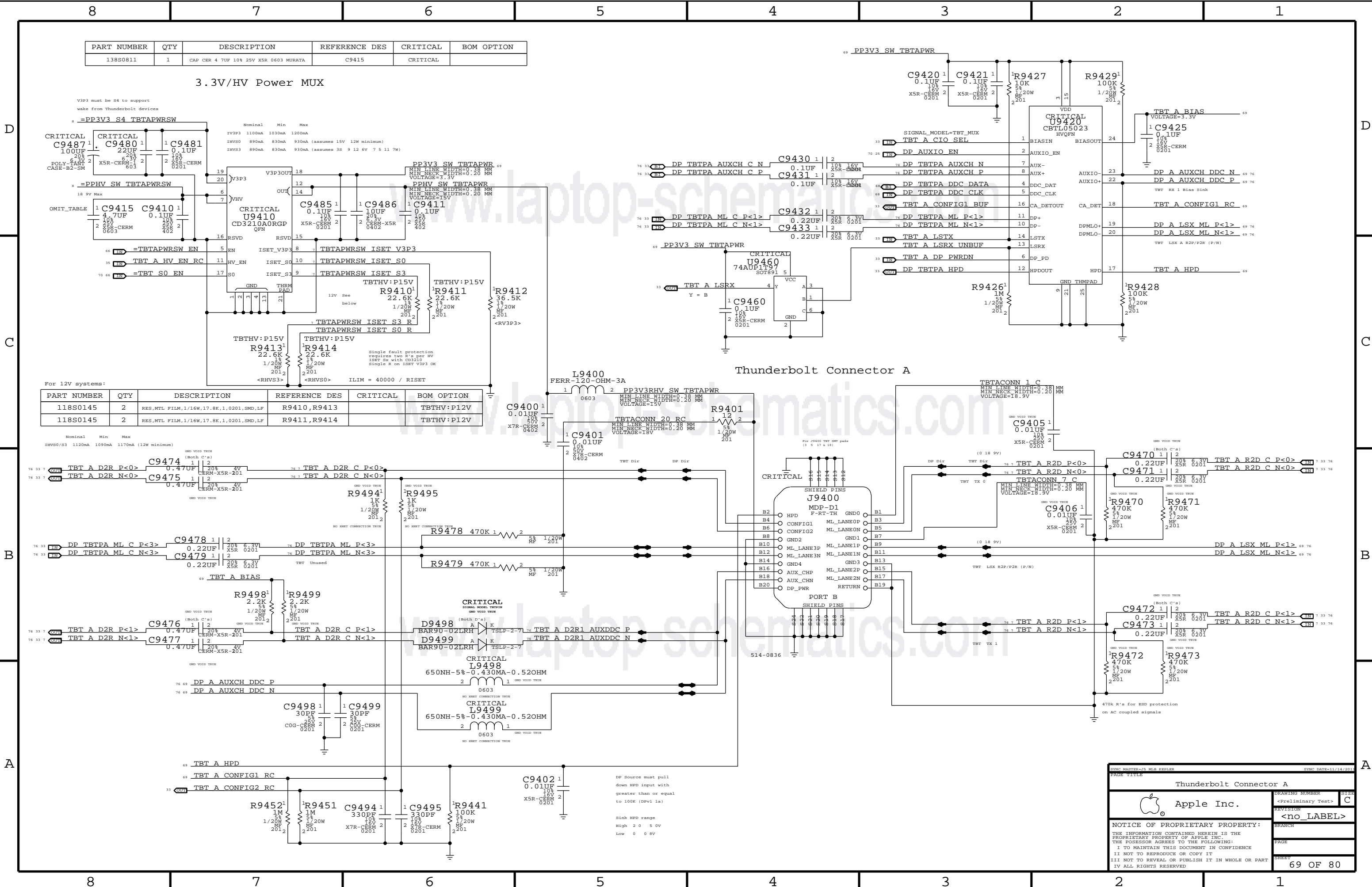


LCD Panel HPD & AUX strapping

SYNC MASTER=DL SENSORS		SYNC DATE=07/11/2015	
PAGE TITLE		eDP Display Connector	
Apple Inc.		DRAWING NUMBER	SIZE
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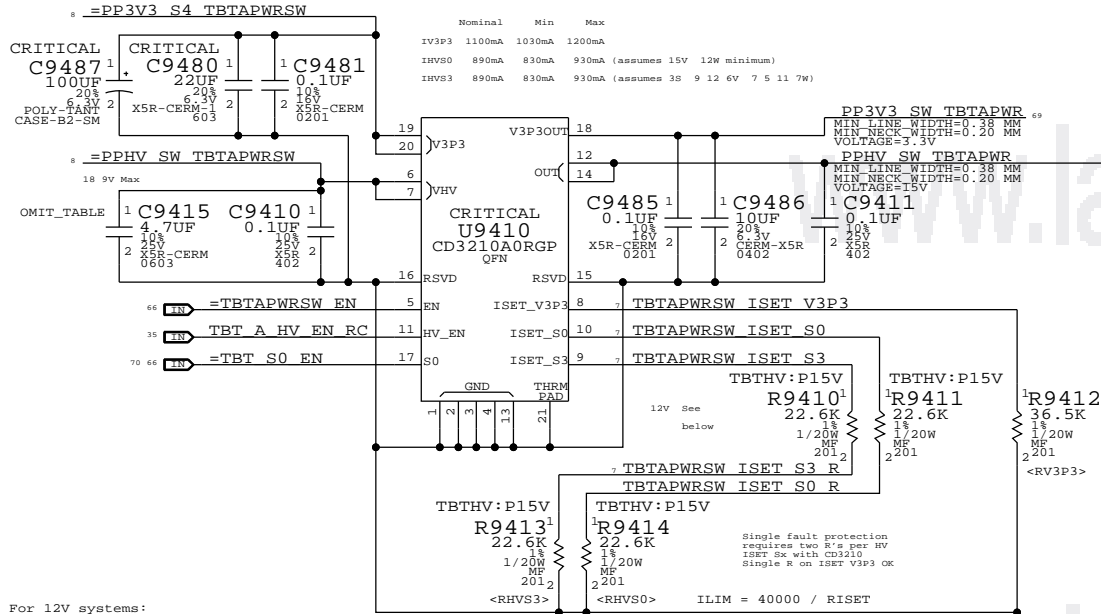
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DDC Crossbar			
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		PAGE	
		SHEET	68 OF 80



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP CER 4 7UF 10% 25V X5R 0603 MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

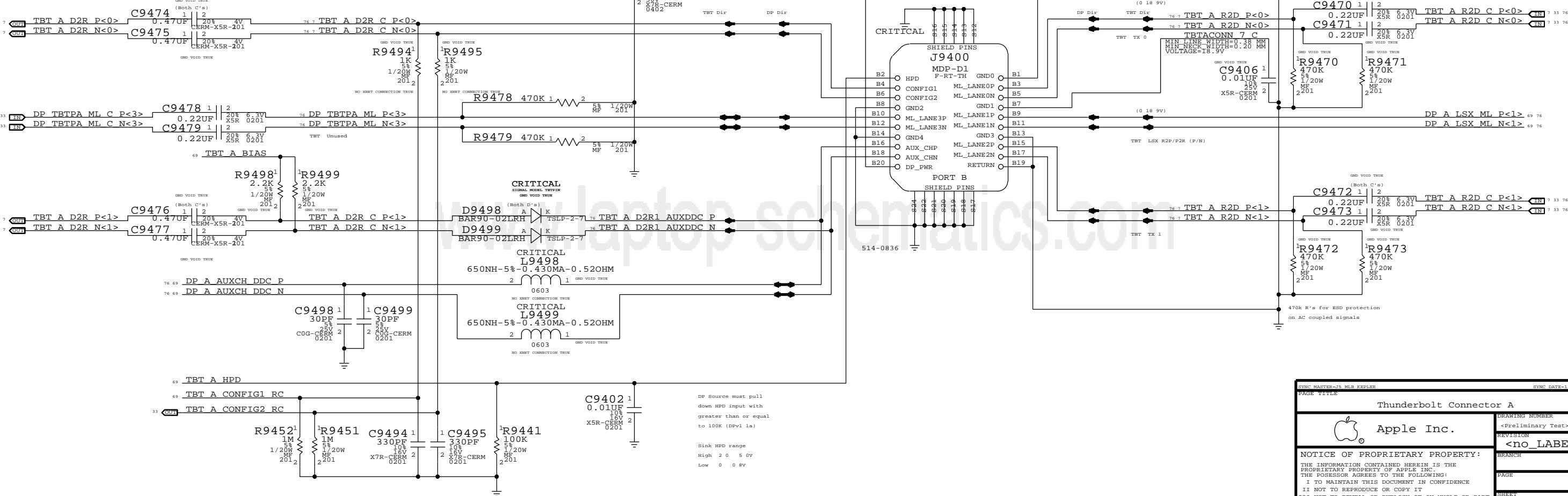
V3P3 must be S4 to support wake from Thunderbolt devices



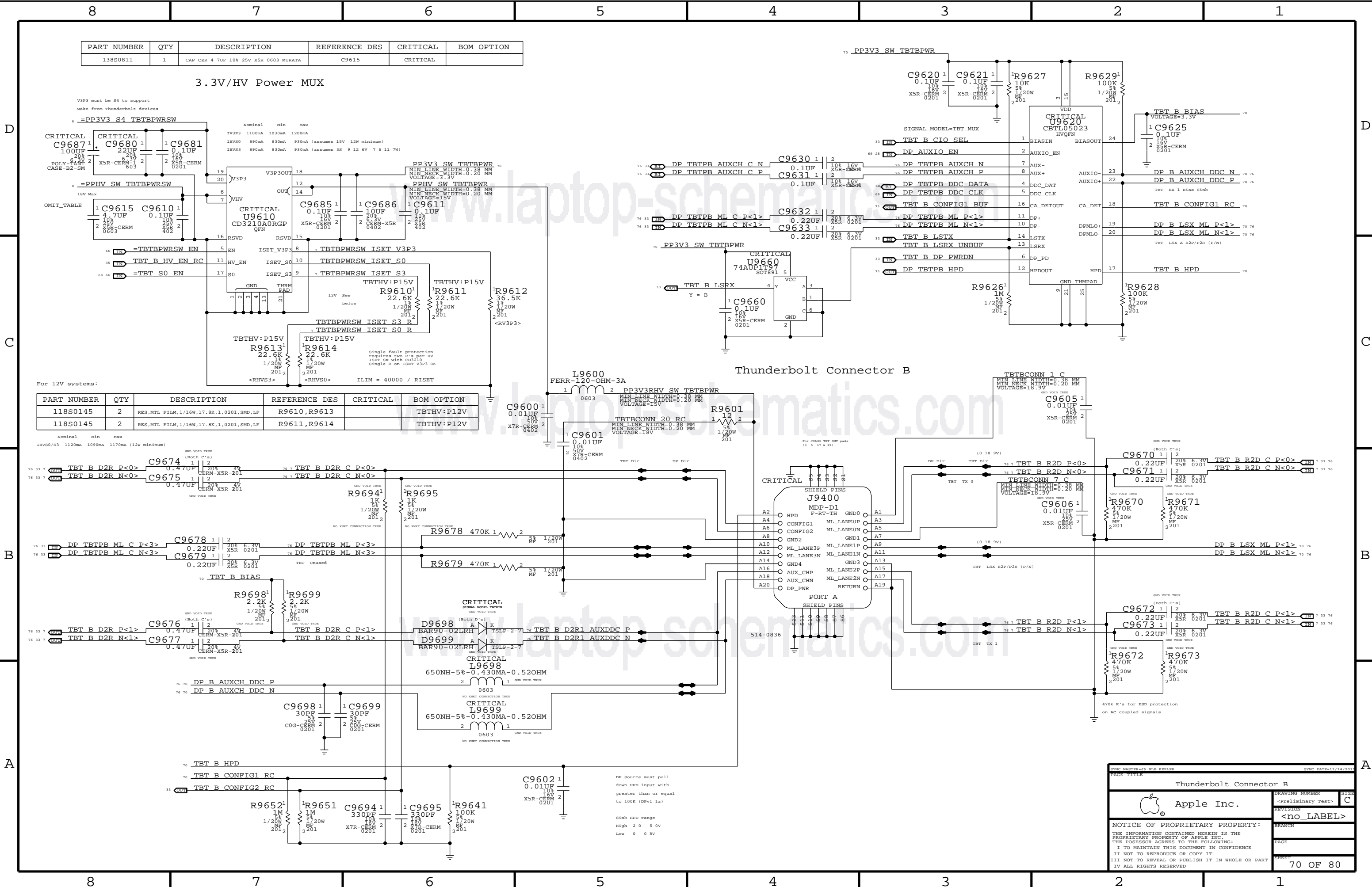
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)



SYNCH WATERSHED MIB EXPLORER		SYNCH DATE:11/14/2011	
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Thunderbolt Connector A		DRAWING NUMBER	SIZE
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CPU Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	=4X_DIELECTRIC	?
CPU_ITP	*	=4x_DIELECTRIC	?
CPU_VCCSENSE	*	=6X_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.












SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X DIELECTRIC	?
CLK PCIE	*	=5X DIELECTRIC	?


CPU Net Properties

ELECTRICAL_CONSTRAINT_SET		NET TYPE			
		PHYSICAL	SPACING		
	DMT_S2N	PCIE_85D	PCIE	DMI S2N P<3:0>	7 10 18
	DMT_S2N	PCIE_85D	PCIE	DMI S2N S<3:0>	7 10 18
	DMT_N2S	PCIE_85D	PCIE	DMI N2S P<3:0>	7 10 18
	DMT_N2S	PCIE_85D	PCIE	DMI N2S N<3:0>	7 10 18
	FDI_DATA	PCIE_85D	PCIE	FDI DATA P<7:0>	7 10 18
	FDI_DATA	PCIE_85D	PCIE	FDI DATA N<7:0>	7 10 18
	FDI_FSYNC	CPU_50S	CPU AGTL	FDI_FSYNC<1..0>	10 18
	FDI_LSYNC	CPU_50S	CPU AGTL	FDI_LSYNC<1..0>	10 18
	FDI_INT	CPU_50S	CPU AGTL	FDI_INT	10 18
	DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M CPU P	7 11 17
	DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M CPU N	7 11 17

CPH_EDP_COMP	CPH_27P4S	CPH_COMP	CPU_EDP_COMP	10
CPH_PEG_COMP	CPH_27P4S	CPH_COMP	CPU_PEG_COMP	10
CPH_CFG	CPH_50S	CPH_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPH	CLK_BCTE_90D	CLK_BCTE	ITPCPU CLK100M_P	11 17
XDP_CLK_CPH	CLK_BCTE_90D	CLK_BCTE	ITPCPU CLK100M_N	11 17
XDP_CLK_PCH	CLK_BCTE_90D	CLK_BCTE	ITPXDP CLK100M_P	17 24
XDP_CLK_PCH	CLK_BCTE_90D	CLK_BCTE	ITPXDP CLK100M_N	17 24
DPILL_REF_CLK120M	CLK_BCTE_90D	CLK_BCTE	DPILL_REF CLK_P	11 17
DPILL_REF_CLK120M	CLK_BCTE_90D	CLK_BCTE	DPILL_REF CLK_N	11 17
XDP_TDI	CPH_50S	CPH_ITP	XDP CPU TDI	11 24
XDP_TDO	CPH_50S	CPH_ITP	XDP CPU TDO	11 24
XDP_TMS	CPH_50S	CPH_ITP	XDP CPU TMS	11 24
XDP_TCK	CPH_50S	CPH_ITP	XDP CPU TCK	11 24
XDP_TRST_L	CPH_50S	CPH_ITP	XDP CPU TRST_L	11
XDP_BPM	CPH_50S	CPH_ITP	XDP BPM L<3..0>	11 24
XDP_BPM_L	CPH_50S	CPH_ITP	XDP BPM L<7..4>	11 24
XDP_BDRESET_L	CPH_50S	CPH_ITP	XDP DBRESET_L	11 24 25
XDP_PRDY_L	CPH_50S	CPH_ITP	XDP CPU PRDY_L	11 24
XDP_PREQ_L	CPH_50S	CPH_ITP	XDP CPU PREQ_L	11 24
CPH_CATERR_L	CPH_50S	CPH_AGTL	CPU CATERR_L	11 39
CPH_PROC_SEL_L	CPH_50S	CPH_AGTL	CPU PROC_SEL_L	11 20
CPH_PECI	CPH_50S	CPH_VID	CPU PECI	11 20
CPH_PROCHOT_L	CPH_50S	CPH_AGTL	CPU PROCHOT_L	11 39 40
XDP_CPH_PWRGD	CPH_50S	CPH_ITP	XDP CPU_PWRGD	24
PM_THRMTRIP_L	CPH_50S	CPH_8MIL	PM_THRMTRIP_L	11 20 40
PM_SYNC	CPH_50S	CPH_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPH_50S	CPH_AGTL	PM_MEM_PWRGD	11 18 27
CPH_PWRGD	CPH_50S	CPH_AGTL	CPU_PWRGD	11 20 24
CPH_SM_RCOMP	CPH_27P4S	CPH_COMP	CPU_SM_RCOMP<2..0>	11
	CPH_50S	CPH_VID	CPU_VIDSOUT	13 61
	CPH_50S	CPH_VID	CPU_VIDSCLK	13 61
	CPH_50S	CPH_VID	CPU_VIDALERT_L	13 61
	CPH_55S	CPH_VID	CPU_VCCSA_VID<1..0>	13 58
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_VCCSENSE_P	13 61
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_VCCSENSE_N	13 61
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_VCCIOSENSE_P	13 63
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_VCCIOSENSE_N	13 63
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_AXG_SENSE_P	13 61
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_AXG_SENSE_N	13 61
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_VCC_VALSENSE_P	10
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_VCC_VALSENSE_N	10
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_AXG_VALSENSE_P	10
CPH_VCCSENSE	CPH_27P4S	CPH_VCCSENSE	CPU_AXG_VALSENSE_N	10
CPH_VCCSASENSE	CPH_50S	CPH_AGTL	CPU_VCCSASENSE	13 58

00	CPU_MEM_VREF		CPU_VREF	PCPU MEM VREFD0 A	10 31
00	CPU_MEM_VREF		CPU_VREF	PCPU MEM VREFD0 B	10 31
00	CPU_MEM_VREF		CPU_VREF	PP0V75 S3 MEM VREFD0 A	28 31
00	CPU_MEM_VREF		CPU_VREF	PP0V75 S3 MEM VREFD0 B	28 31
00	CPU_MEM_VREF		CPU_VREF	PP0V75 S3 MEM VREFCA A	28 31
00	CPU_MEM_VREF		CPU_VREF	PP0V75 S3 MEM VREFCA B	28 31
00	XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M P	24
00	XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M N	24

XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M P
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M N

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CPU Constraints			
		DRAWING NUMBER <Preliminary Test>	
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LPC Bus Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CLK LPC 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
LPC	*	6 MIL	?				
CLK LPC	*	8 MIL	?				
SMBus Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
SMB	*	=2x DIELECTRIC	?				
HD Audio Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
HDA	*	=2x DIELECTRIC	?				
SIO Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
CLK SLOW	*	8 MIL	?				
SPI Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
SPI	*	8 MIL	?				
PCH Net Properties							
ELECTRICAL_CONSTRAINT_SET				NET TYPE		SPACING	
				PHYSICAL			
LPC_AD	LPC 50S	LPC	LPC AD<3..0>			7 17 39 41	
LPC_FRAME_L	LPC 50S	LPC	LPC FRAME L			7 17 39 41	
LPC_RESET_L	LPC 50S	LPC	LPC RESET L			25	
PCH_LPC_CLK0	CLK LPC 50S	CLK LPC	LPC CLK33M SMC R			19 25	
CLK_LPC_50S	CLK LPC 50S	CLK LPC	LPC CLK33M SMC			7 25 39	
CLK_LPC_50S	CLK LPC 50S	CLK LPC	LPC CLK33M LPCPLUS			7 25 41	
SMBUS_PCH_CLK	SMB 50S	SMB	SMBUS_PCH_CLK			7 17 42	
SMBUS_PCH_DATA	SMB 50S	SMB	SMBUS_PCH_DATA			7 17 42	
SMBUS_PCH_0_CLK	SMB 50S	SMB	SML_PCH_0_CLK			17 42	
SMBUS_PCH_0_DATA	SMB 50S	SMB	SML_PCH_0_DATA			17 42	
SMBUS_SMC_1_S0_SCL	SMB 50S	SMB	SML_PCH_1_CLK			17 42	
SMBUS_SMC_1_S0_SDA	SMB 50S	SMB	SML_PCH_1_DATA			17 42	
HDA_BIT_CLK	HDA 50S	HDA	HDA_BIT_CLK			17 61	
HDA_BIT_CLK_R	HDA 50S	HDA	HDA_BIT_CLK_R			17	
HDA_SYNC	HDA 50S	HDA	HDA_SYNC			17 61	
HDA_SYNC_R	HDA 50S	HDA	HDA_SYNC_R			17	
HDA_RST_L	HDA 50S	HDA	HDA_RST_R_L			17	
HDA_RST_L	HDA 50S	HDA	HDA_RST_L			17 61	
HDA_SDIN0	HDA 50S	HDA	HDA_SDIN0			17 61	
AUD_SDI_R	HDA 50S	HDA	AUD_SDI_R			61	
HDA_SDOUT	HDA 50S	HDA	HDA_SDOUT			17 61	
HDA_SDOUT_R	HDA 50S	HDA	HDA_SDOUT_R			17 25	
SPI_CLK	SPI 55S	SPI	SPI_CLK_R			17 41	
SPI_CLK	SPI 55S	SPI	SPI_CLK			41	
SPI_MOSI	SPI 55S	SPI	SPI_MOSI_R			17 41	
SPI_MOSI	SPI 55S	SPI	SPI_MOSI			41	
SPI_MISO	SPI 55S	SPI	SPI_MISO			17 41	
SPI_CS0	SPI 55S	SPI	SPI_CS0_R_L			17 41	
SPI_CS0	SPI 55S	SPI	SPI_CS0_L			41	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P			7 17 36	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N			7 17 36	
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P			7 17 36	
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N			7 17 36	
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P			7 36	
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N			7 36	
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P			7 17 36	
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N			7 17 36	
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P			7 17 36	
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N			7 17 36	
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P			7 36	
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N			7 36	
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P			7 36	
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N			7 36	
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P			7 17	
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N			7 17	
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P			7 17 33	
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N			7 17 33	
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P			17	
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N			17	
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P			7 17	
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N			17	
CPU_50S	CLK_PCIE		PCH_CLK14P3M_REFCLK			17	
CPU_50S	CLK_PCIE		PCH_CLK33M_PCIIN			7 17 25	
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P			7 9 17	
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N			7 9 17	
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P			7 9 17	
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N			7 9 17	
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P			7 17 36	
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N			7 17 36	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P			7 17 36	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N			7 17 36	
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P			7 9 17	
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N			7 9 17	
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P			7 17	
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N			7 17	
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>			7 9 33	
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>			7 9 33	
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>			7 33	
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>			7 33	
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>			7 9 33	
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>			7 9 33	
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>			7 33	
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>			7 33	

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C							C
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A							A
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	= 2:1_SPACING	?
THERM	*	= 2:1_SPACING	?
AUDIO	*	= 2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	CPUTHMSNS D2 P 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	CPUTHMSNS D2 N 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	CPU THERMD P 9 10
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	CPU THERMD N 9 10
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	GPUTHMSNS D P 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	GPUTHMSNS D N 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	GPU TDIODE P 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	GPU TDIODE N 46
4600	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	TBT THERMD P 46
4600	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	TBT THERMD N 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	DDR3THMSNS D1 P 46
	SENSE_DIFFPAIR	THERM 1T01 55S	THERM	DDR3THMSNS D1 N 46
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	CPUVCCIOS0 CS P 43 63
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	CPUVCCIOS0 CS N 43 63
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	CPU VDDQ SENSE P 13
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	CPU VDDQ SENSE N 13
4600	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCD PANEL P 43
4600	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCD PANEL N 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V35 S3 MEM P 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V35 S3 MEM N 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS SSD P 37 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS SSD N 37 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 3V3 S0 SSD R P 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 3V3 S0 SSD R N 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS WLAN P 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS WLAN N 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCDBKIT P 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCDBKIT N 43
4600	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS TBT P 80
4600	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS TBT N 80
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V35 S3 MEM R P 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V35 S3 MEM R N 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	VCCSA50 CS P 58 80
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	VCCSA50 CS N 58 80
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	
4635	HDMI_CLK	HDMI_90D	HDMI	HDMI IG CLK C P 7 9 36
4635	HDMI_CLK	HDMI_90D	HDMI	HDMI IG CLK C N 7 9 36
4635	HDMI_DATA	HDMI_90D	HDMI	HDMI IG DATA C P<2..0> 7 9 36
4635	HDMI_DATA	HDMI_90D	HDMI	HDMI IG DATA C N<2..0> 7 9 36

D1 Specific Net Properties


ELECTRICAL_CONSTRAINT_SET		NET TYPE			
		PHYSICAL	SYMBOL	SPACING	
	PCIE CLK100M AP	CLK PCIE 90D	CLK PCIE	PCIE CLK100M AP CONN P	7 36
	PCIE CLK100M AP	CLK PCIE 90D	CLK PCIE	PCIE CLK100M AP CONN N	7 36
		1T01 DIFFPAIR		CHGR CSI R P	57
		1T01 DIFFPAIR		CHGR CSI R N	57
		1T01 DIFFPAIR		CHGR CSO R P	57
		1T01 DIFFPAIR		CHGR CSO R N	57
	USB_RT	USB_R5D	USB	USB BT CONN P	36
	USB_RT	USB_R5D	USB	USB BT CONN N	36
	USB_RT	USB_R5D	USB	USB BT WAKE P	36
	USB_RT	USB_R5D	USB	USB BT WAKE N	36
	AUDIO DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN SL OUT P	7 53 55
	AUDIO DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN SL OUT N	7 53 55
	AUDIO DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN SR OUT P	7 53 55
	AUDIO DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN SR OUT N	7 53 55
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN L OUT P	7 53 55 78
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN L OUT N	7 53 55 78
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN R OUT P	7 53 55 78
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN R OUT N	7 53 55 78
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNSG P	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNSG N	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS1G P	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS1G N	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS2G P	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS2G N	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISUMG R P	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISUMG R N	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HS OTHER P	44
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HS OTHER N	44
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HS COMPUTING P	44
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HS COMPUTING N	44
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS P	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS N	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS1 P	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS1 N	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS2 P	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISNS2 N	43 62
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISUM R P	43
	SENSE DIFFPAIR	SENSE 1T01 55S	SENSE	CPUIMVP ISUM R N	43
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L01 L P	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L01 L N	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L01 R P	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L01 R N	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L02 L P	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L02 L N	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L02 R P	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD L02 R N	51 53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD MIC INL P	51 54
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD MIC INL N	51 54
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP LIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP LIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP RIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP RIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP LSUBIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP LSUBIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP RSUBIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD SPKRAMP RSUBIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP LIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP LIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP RIN P	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP RIN N	53
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	HS MIC HI RC	54
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	HS MIC LO RC	54
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	HS MIC HI	54
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	HS MIC LO	54
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN L OUT P	7 53 55 78
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN L OUT N	7 53 55 78
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN R OUT P	7 53 55 78
	AUDIO DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN R OUT N	7 53 55 78
	USB_TP4D	USB_R5D	USB	USB TP4D R P	26 47
	USB_TP4D	USB_R5D	USB	USB TP4D R N	26 47
	USB_HUB	USB_R5D	USB	PU USBHUB DN4 P	9
	USB_HUB	USB_R5D	USB	PU USBHUB DN4 N	9
		SR_POWER		PP3V3_S5	7 8
		SR_POWER		PP3V3_S0	7 8
		SR_POWER		PPIV5_S3RS0_CPUDDR	8
		GND		GND	

DDR3 Loaded Segment Constraint Relaxations
Alternate single ended and differential impedances between devices.

Graphics ,SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

SYNC MASTER=J5 MLB		SYNC DATE=07/29/2011	
PAGE TITLE			
Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER <Preliminary Test>	SIZE C
		REVISION <no_LABEL>	
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8	7	6	5	4	3	2	1
D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA, BGA_MEM		MM	16.2
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP, BOTTOM	0.1 MM	?
1:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.1 MM	?
1:1_SPACING	ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

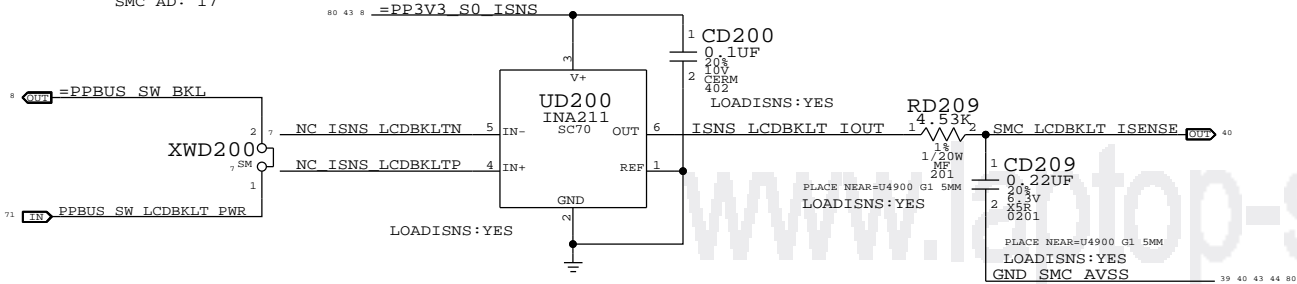
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET			NET TYPE		
			PHYSICAL	SPACING	
660	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 33
661	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 33
662	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 33
663	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 33
664	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 33
665	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 33
666	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 33
667	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 33
668	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	33
669	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	33
670	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	33
671	DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	33
672	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	33
673	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	33
674	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	33
675	DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	33
676	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	9 67
677	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	9 67
678	DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	9 67
679	DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	9 67
680	DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 67
681	DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 67
682	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67
683	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67
684	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	
685	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	
686	USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_P	7 36
687	USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_N	7 36
688	USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_F_P	7 36
689	USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_F_N	7 36
690	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
691	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
692	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
693	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
694	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
695	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
696	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
697	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
698	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
699	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
690	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
691	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
692	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
693	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
694	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
695	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36
696	USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
697	USB3_EXTB_TX				

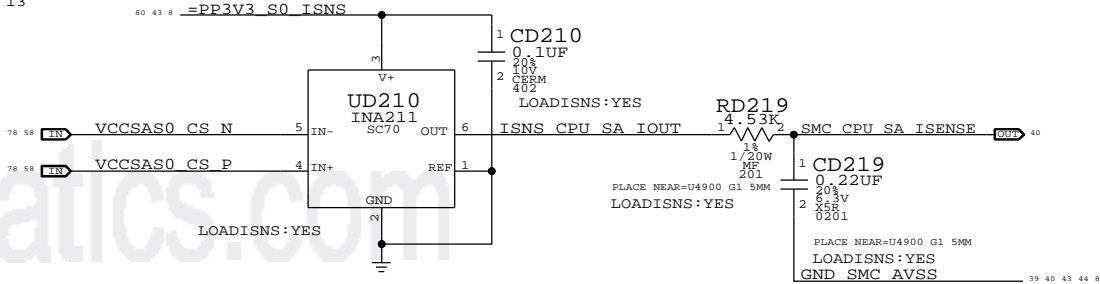
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



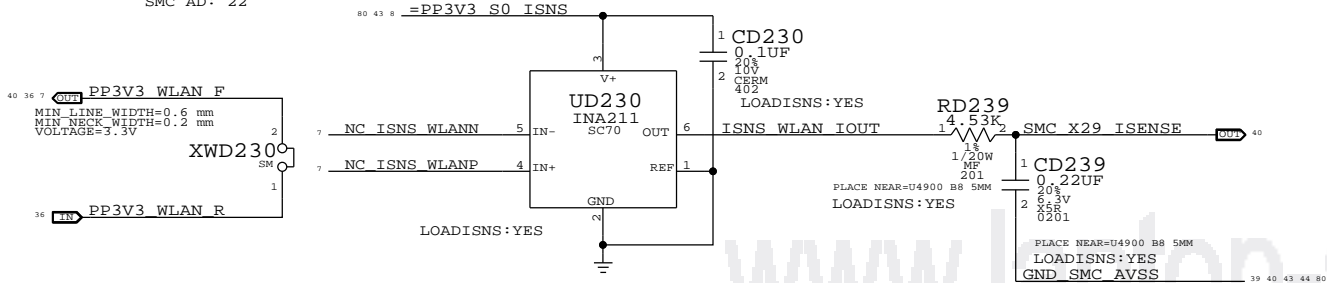
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



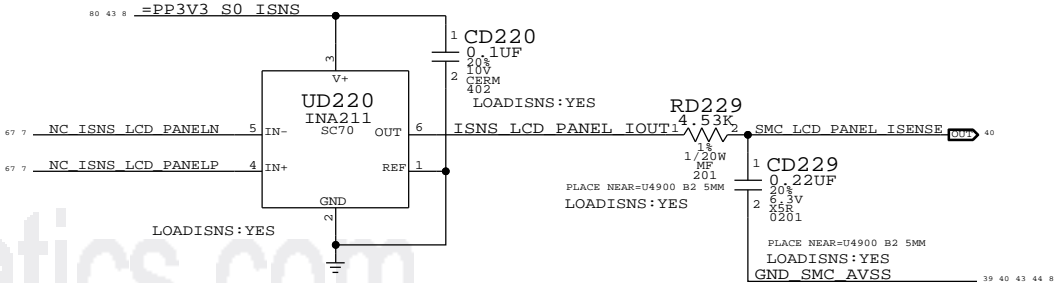
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



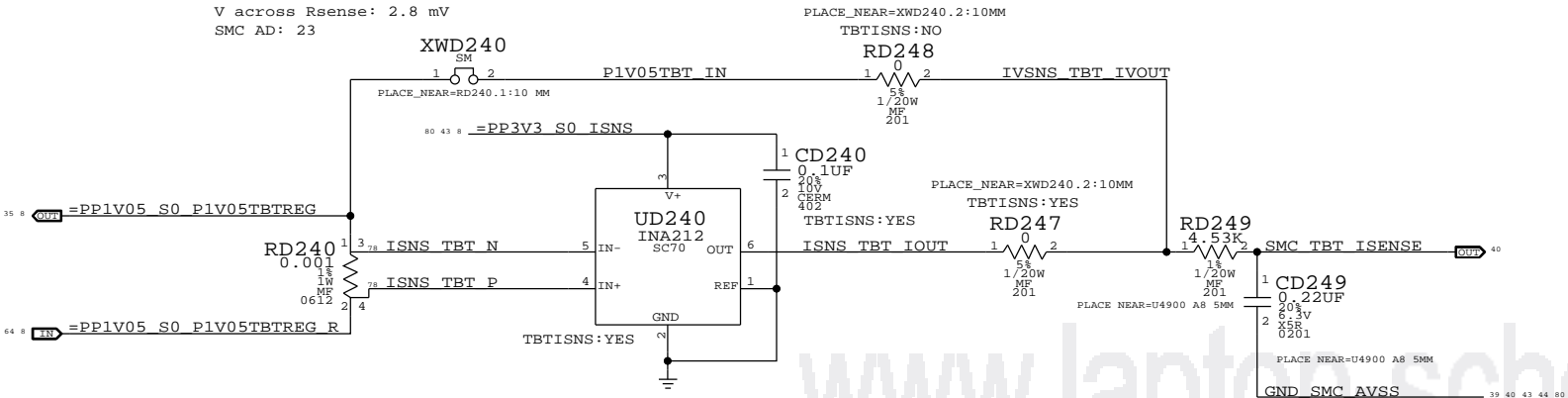
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



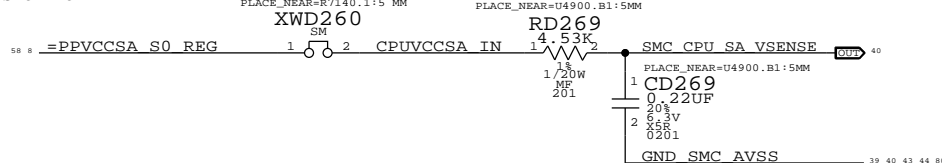
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



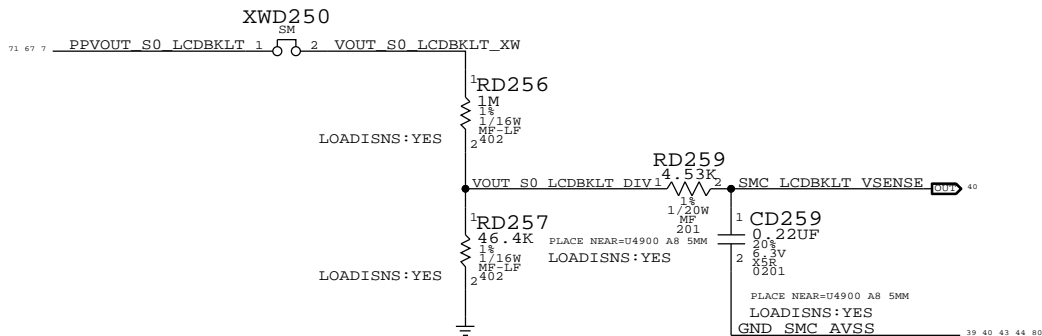
CPU SA Voltage Sense (VC2C)

Gain: 1x
SMC ADC: 14



LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

SYMC PARTS-CD SENSORS		SYMC DATE=07/11/2011	
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